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Characterization and Utilization of 600 V GaN GITs for 4.5 kW Single Phase Inverter Design

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To the Graduate Council:

I am submitting herewith a thesis written by Paige Williford entitled "Characterization and Utilization of 600 V GaN GITs for 4.5 kW Single Phase Inverter Design." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

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Characterization and Utilization of 600 V GaN GITs for 4.5 kW Single Phase Inverter Design

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Abstract

The Gallium Nitride, high electron mobility transistor (GaN HEMT) has emerged as a promising replacement to Silicon (Si) in high-frequency applications, where its superior properties allow for faster switching and higher power density converters. However, the fast switching capability of GaN, while theoretically beneficial to converter design, presents several challenges due to the presence of printed circuit board (PCB) and device parasitics. Therefore, it is imperative that the results of device characterization reflect actual device behavior in order to adequately model the device for converter design.

This thesis focuses on characterization and utilization of 600 V/30 A Gallium Nitride gate injection transistors, or GaN GITs. The experimental data from static and dynamic characterization was used to maximize the performance of the devices in each phase leg of a 4.5 kW, single-phase, full-bridge inverter. The impact of PCB and device parasitics on switching behavior was also investigated, and a trade-off study of switching loss, overshoot voltage, and dead time loss is presented. Device packaging is also of interest regarding the design of high-frequency devices. This thesis compares the impact of two package designs for the GIT device by designing two separate inverters with the same specifications utilizing the different packages.

Finally, due to the lower critical energy of the GaN HEMT during a short circuit, this thesis studies the short-circuit robustness of the devices. The performance of a unique gate sensing protection scheme is compared between two different packages, and the impact of the gate drive and protection circuit design parameters on performance is evaluated.

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Chapter 1

Introduction

1.1 Motivation

As stricter operating requirements of power converters, such as temperature, size and power rating, enforce new constraints on converter design (e.g., higher power density, faster switching frequency, etc.), improvements in both converter design and the power switching devices themselves are increasingly important. Compared to traditional Silicon devices, the advent of wide bandgap devices such as SiC and GaN offers a potential to meet these emerging operational needs, but the unique properties of these devices present a new challenge in converter design and require improved characterization techniques, PCB layout design, and parasitics and device models [1] [2, 3].

While GaN in comparison to Si and SiC has a higher electric breakdown field, devices are typically manufactured in the 600/650 V range due to limitations in the manufacturing process. Without improved methods of growing GaN-on-GaN substrates, the majority of commercially available GaN devices are lateral structures, referred to as high electron mobility transistors, or HEMTs. Figure 1.1 is an example of a typical HEMT structure. A region of high-mobility electrons is formed at the heterojunction of the AlGaN/GaN barrier due to the effect of piezoelectric polarization. This channel is commonly referred to as the two dimensional electron gas, or (2DEG), and creates a low-resistance path from drain to source, making the device inherently depletion-mode or normally “on.” This means that the device requires a negative gate bias to remain off, which is an undesirable property in regards to voltage source converter design.

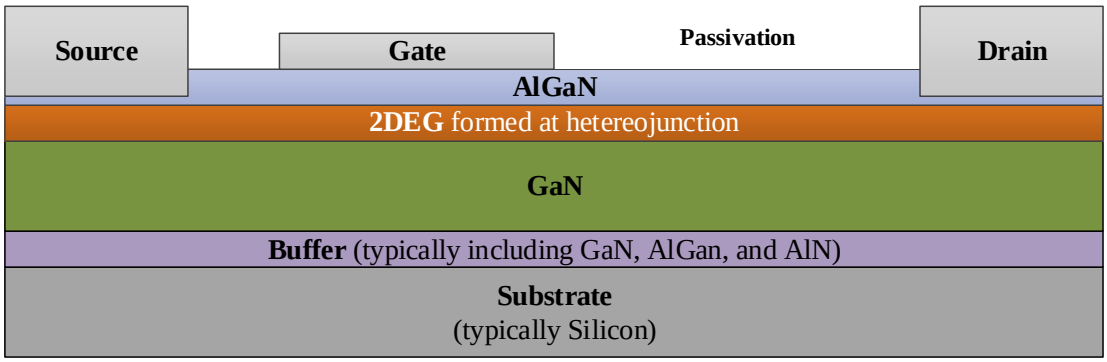


Figure 1.1. Basic structure of depletion-mode GaN HEMT.

There have been several structures developed to make the HEMT an enhancement-mode device, such as plasma treated gate, recessed gate, insulated gate, and p-doped GaN or AlGaN gate [4]. This thesis specifically studies the characterization and application of the non-insulated, enhancement mode GaN HEMT, known as the gate injection transistor (GIT), in the design of a 4.5 kW inverter. The GIT is unique in that there exists a p-doped AlGaN or GaN cap beneath the gate, lifting the threshold to a positive voltage. This p-doped layer results in a diode-like characteristic, which requires a sufficient amount of gate current to forward bias and enhance the depleted 2DEG channel, typically in the mA range. The forward voltage of the internal gate diode is clamped to 3-5 V depending on the manufacturer and gate current, making the gate characteristic of the GIT similar to the I-V characteristic of a conventional p-n diode. Panasonic is the first manufacturer to develop the GIT [5], the structure of which is shown in Figure 1.2 and the operation shown in Figure 1.3 and Figure 1.4.

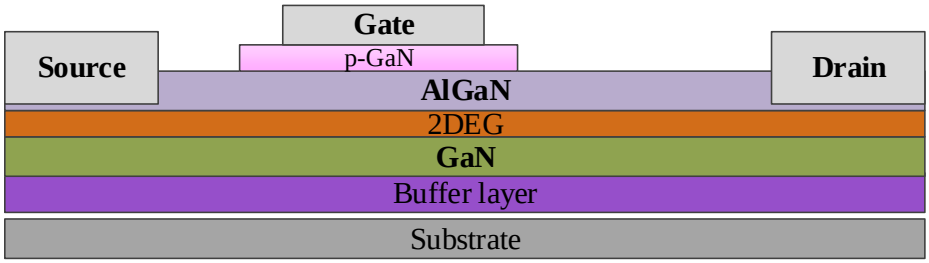


Figure 1.2. Basic structure of an enhancement-mode GaN GIT.

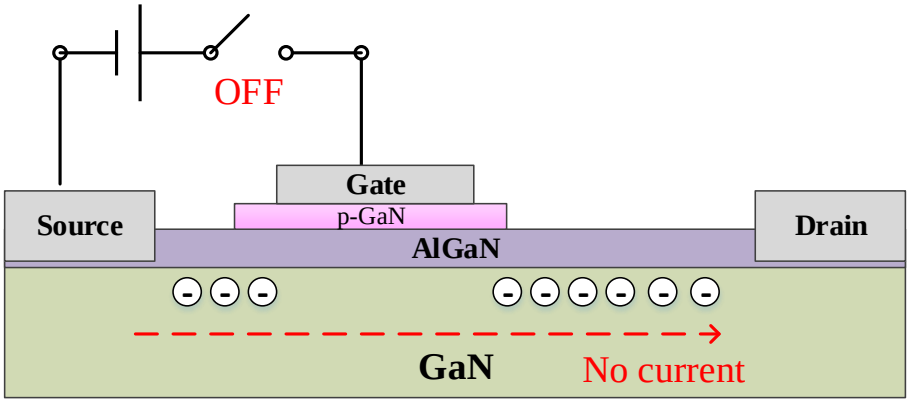


Figure 1.3. GIT operation with V_{gs} = 0 V. p-GaN gate depletes channel under gate.

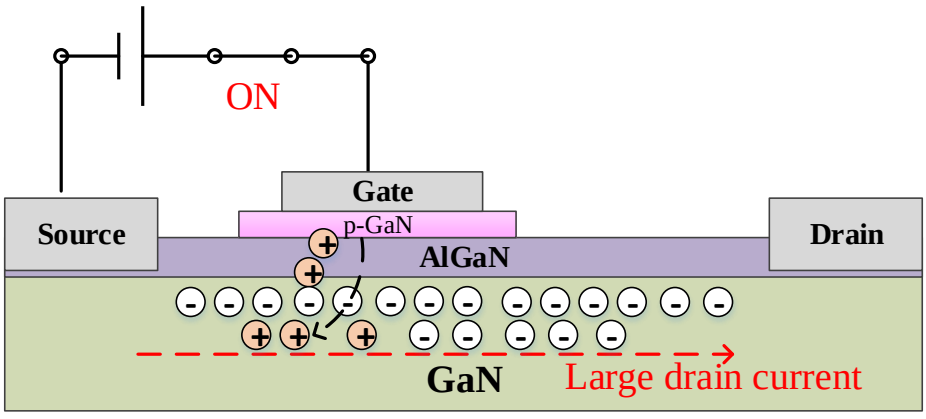


Figure 1.4. GIT operation with $V_{gs} > V_f$. Injected holes increase drain current through conductivity modulation.

In comparison to other HEMT structures, minority carriers are injected into the 2DEG channel after the gate diode exceeds the forward voltage, V_f, further enhancing the conductivity of the 2DEG and reducing the on-resistance [6]. Studies have shown how the GIT can achieve higher saturation current than that of other structures due to this hole injection, and little to no dynamic R_{dson} up to its rated voltage is observed even without double gate contacts [5, 7, 8]. In [9], an 850 V GIT with an additional p-GaN region electrically connected to the drain was shown to completely eliminate R_{dson} for voltages even above the rated voltage by releasing trapped charges near the drain. Some insulated gate structures, such as metal insulator HEMT (MISHEMT), show hysteresis after applying a positive gate bias because of the trapped charges at the at the gate dialectric/GaN interface due to defects. The GIT on the other hand shows no such hysteresis [8]. Compared to insulated gate structures, the GaN GIT has higher saturation current and a lower increase in R_{dson} for similar die size as junction temperature increases. Insulated gate structures are also very sensitive to overvoltage, with a typical maximum gate voltage of less than 10 V, while the GIT has no maximum positive gate voltage. Rather, there is maximum gate current, ~2 A [10].

A downside of the GIT compared to an insulated gate structure is the higher gate drive loss due to the required steady-state gate current [11] and the small margin to increase threshold voltage due to the limitation of the p-n junction barrier height [6]. An additional downside of the GIT is that the recovery of the gate diode during turn-off makes the turn-off delay time slightly longer than the turn-on delay. Despite its disadvantages, the unique properties of the GIT p-doped gate present a unique opportunity to explore new methods

of gate driving beyond the conventional voltage driven method, which carries with it several advantages.

In the GIT, the gate voltage is proportional to the gate current, a constant gate current is required to maintain the gate's forward bias, V_f, and fully enhance the channel. However, it is also desirable to deliver a higher gate voltage in the beginning of the transient for fast turn-on and lower switching loss while maintaining a lower voltage during steady-state to prevent damage of the gate. This makes a more simplified gate drive scheme possible, where a high transient pulse of current is supplied simply by tuning external gate drive parameters instead of designing complicated, multi-level voltage gate drivers. A summary of advantages and challenges of GIT compared to other structures is shown in Table 1.1.

Table 1.1. Comparison of Normally-off AlGaN/GaN FETs [12-16].

	A-PLANE FET	**PLASMA GATE**	**MIS-HEMT**	**GIT**
Advantages	Simple structure Simple process	Low leakage current Controllability of V_{th}	Low leakage current Large I_{max}	No max. positive V_{gs} High I_{max} No current collapse
Challenges	Epitaxial growth No polarization induced charge Increasing I_{max}	Stability of doped fluorine Etching depth	Controllability of V_{th} Stability of insulator/semi-conductor interface	Complexity of gate drive Controllability of V_{th}

The motivation for this work is to characterize 600 V/30 A GaN GITs utilizing a capacitive gate drive scheme that delivers a high pulse of gate current in the beginning of the transient and a small gate current during steady-state. Because the turn-on time is now dependent on both a turn-on gate resistance and a series capacitance, it is important to study the relationship of these parameters on overshoot voltage and switching loss and to study the interaction of these parameters with PCB and device parasitics. This data is also used in the design of a 4.5 kW inverter for photovoltaic applications, with the motivation of understanding the impact factors of the GaN GIT, including the gate driver design, dead time setting, and short-circuit behavior, which are all relevant to other hard-switching GaN-based converters. Two designs are developed utilizing two different device packages to study the impact of package parasitics and PCB layout on the performance of the inverter. Accordingly, an optimized combination of gate drive parameters is proposed based on the trade-off between overshoot voltage and switching loss.

Besides overshoot voltage and switching loss, other unique properties of lateral GaN devices present a challenge in the full-scale inverter design. The dead time behavior, for example, will also have an impact on device performance. Unlike a conventional MOSFET structure, the GIT has no intrinsic body diode to conduct reverse current. Instead, if the gate-drain voltage exceeds the threshold voltage, the channel of the GIT will operate in the third quadrant. This mechanism and the loss induced during the dead time for the 600 V GaN GIT is studied in this thesis, and the impact of the loss on the full scale converter is considered. Additionally, a model for optimal dead time is developed based on the experimental results.

Finally, due to the higher power density and generally smaller die size of GaN, the short circuit robustness is considerably lower than that of Si and SiC devices. Compared to Si, the drift region of GaN devices is designed to take advantage of the high electric field breakdown of GaN material, and therefore, a much higher electric field is to be expected when high drain voltage is applied, leading to higher power dissipation density than Si [6]. Likewise, high short-circuit current is more likely to concentrate in the AlGaN/GaN interface rather than the bulk material of a vertical device, causing extreme localized temperature rise. The higher saturation velocity of GaN also results in higher saturation current, further increasing the likelihood of localized temperature surge during a short-circuit event and consequently leads to lower robustness. Because the converter should be able to successfully withstand a short circuit event with adequate time to detect and turn off the device, the short circuit robustness of the GIT is studied to determine the maximum short circuit withstand time and protection time required. The standard of short-circuit withstand time is typically 10 μs at 50% rated voltage. With this information, the short-circuit failure time is investigated for 600 V/30 A GaN GITs, and the overcurrent protection scheme presented in [17] is verified to protect the devices during a short circuit event over a full operating range. The impact of package parasitics and other parameters on the performance of the protection scheme is also studied.

1.2 Outline of thesis

In Chapter 2, state-of-the-art gate driver schemes for the GaN GIT are presented along with an explanation of the capacitive gate drive design used to deliver dynamic control of gate current for faster transient switching. Challenges and efforts in

characterization of high voltage GaN devices will be discussed, including dead time optimization and loss analysis. Finally, the short-circuit robustness of GaN and overcurrent protection schemes will be presented.

Chapter 3 will cover the characterization results of the 600 V/30 A GITs, including the design of steady-state gate current, trade-off study of overshoot voltage and switching loss, a comparison of performance between two different device packages, and finally observations on discrepancies of voltage overshoot measurement between a prototype full-scale converter and double pulse test (DPT) results.

In Chapter 4, the dead time loss is evaluated for various dead times and operating conditions, and a loss model based on experimental data is developed. The results are verified in the full-scale prototype with the double-pulse test results, and an adaptive dead time model is developed based on sinusoidal load current.

The short circuit robustness of the GaN GIT is discussed in Chapter 5. This includes high temperature short-circuit robustness and detection necessary to protect the devices during a short circuit event during worst case scenario. Impact factors of protection scheme performance are also discussed.

Finally, this thesis will conclude in Chapter 6 with a summary of the work presented and further improvements and future work, which may utilize the findings in this thesis.

Chapter 2

Literature Review

2.1 GaN GIT and gate drive

The steady-state gate current requirement of the GIT presents a unique challenge for gate drive design. It is often desirable to supply a high transient gate voltage in the beginning of the pulse to decrease switching loss, but in order to achieve a high gate voltage pulse in the GIT, a high pulse of gate current is required. An RC network is suggested in [10] by Infineon to solve this problem, and a similar scheme is used with Panasonic's xGaN gate driver [18]. By incorporating a series capacitor with the turn-on resistance, a short burst of gate current is possible during the turn-on transient. A large, parallel turn-on resistor then provides a path for the smaller, steady-state current. An example of this gate drive scheme using all discrete components is shown in Figure 2.1**,** and the gate voltage and current characteristics are shown in Figure 2.2**.**

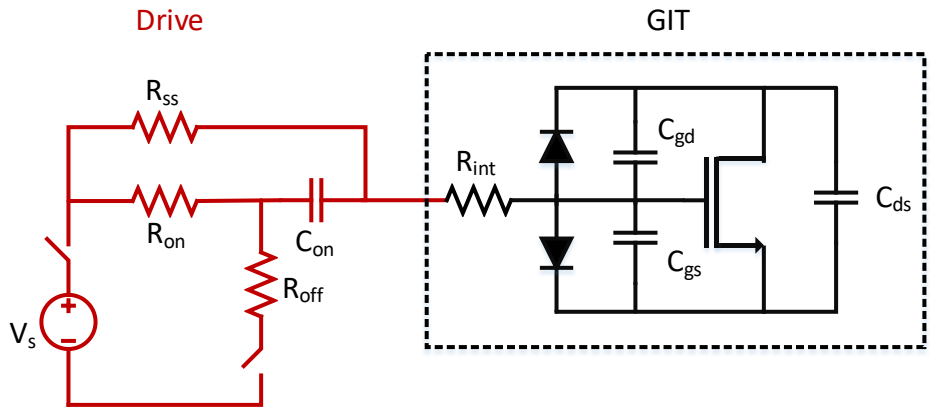


Figure 2.1. Schematic of recommended GIT gate drive circuit.

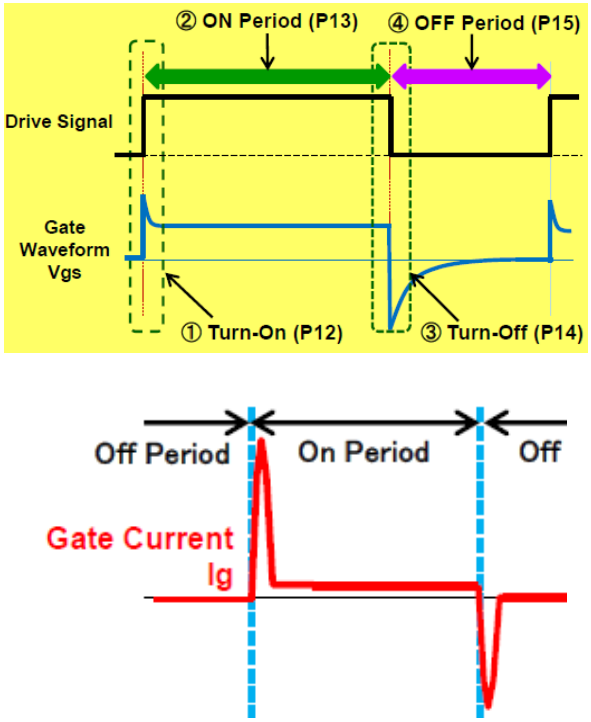


Figure 2.2. Gate voltage and current waveforms utilizing GIT gate drive circuit from Panasonic application note [18].

Before the switching event, C_{on} remains uncharged. After the gate driver voltage changes from zero to V_s, the series and gate-source capacitance is charged until the gate voltage reaches the diode voltage of ~3.5 V (which depends on the constant steady-state gate current). The duration of this first pulse depends on the time constant $R_{on} \cdot C_{on}$. As C_{on} charges, the current through R_{on} falls to zero, and the remaining current is the steady-state gate current of $(V_s\text{-}V_{gs})/R_{ss}$. This current is typically in the milliamp range between 5-50 mA. The parameters V_s, R_{on}, C_s, and R_{ss} can be tuned to produce the desired driving voltage. A separate path is provided for the turn-off gate resistance, which also provides a path to discharge the series gate capacitance. The impact of this capacitance on the shape of the turn-off waveform is also discussed in [10]. Because the voltage across C_s remains the

same before the turn-off transient, the capacitor voltage, V_{cs}, is now applied to the gate in the negative direction even without a bipolar power supply. C_{gs} is then discharged through the gate resistance and the turn-off resistance, with a corresponding time constant. If the voltage is not completely discharged by the end of the duty off-cycle, the V_{gs} will be negative for the subsequent turn-on sequence and induce higher turn-on loss. On the other hand, if the capacitor is discharged too quickly, the device is less robust against high *dv/dt* transients, where the current induced by cross-talk can charge C_{gs} above the threshold voltage and result in shoot-through. A bipolar power supply can overcome this challenge and guarantee the device is robust against dv/dt induced cross-talk at the expense of higher dead-time loss and turn-on switching loss [7].

Some updated versions of the gate drive scheme add modifications to the circuit to avoid the use of bipolar power supply [7], [19]. Shown in Figure 2.3**,** Zener diode, ZD_1, is added in series with the steady-state current limiting resistor, R_3, to avoid complete discharge of C_s. For quick discharging, zener diode ZD_2 and schottky diode SD_s provide a path through the turn-off gate resistance [19]. However, this scheme requires additional

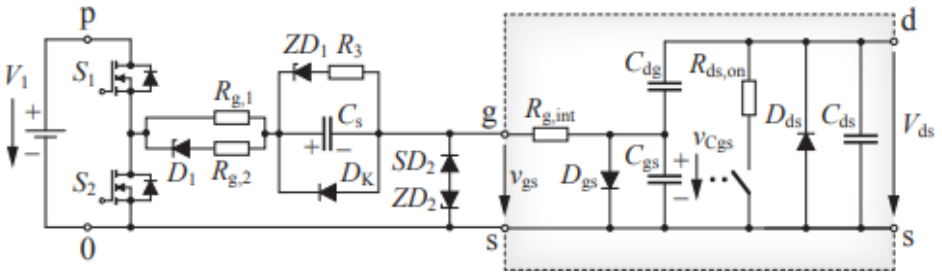


Figure 2.3. Proposed GIT gate drive design for improved performance and protection [19].

components and complexity that shows little benefit against the bipolar scheme in [20]. Panasonic on the other hand has developed a gate driver with integrated components, featuring a built-in negative off-state voltage regulator (independent of the series capacitor and turn-off resistance), active Miller clamping, and an adjustable constant-current source for the steady-state turn-on output. The presence of the built-in negative gate voltage regulator eliminates the need for a split supply voltage and is easily tunable via the external resistor. The external series gate capacitor is still required, however, to provide the high initial pulse of gate current. This x-GaN driver has been released commercially, and a circuit diagram from its datasheet is shown in Figure 2.4, with *Out 1* supplying the initial voltage V_{cc}, which charges the capacitor C_s, supplying a high transient gate current. At the same time, *Out 2* sources the smaller, constant gate current, *IG*, controlled by an external resistor, which maintains the forward diode voltage during the remainder of the "on" time.

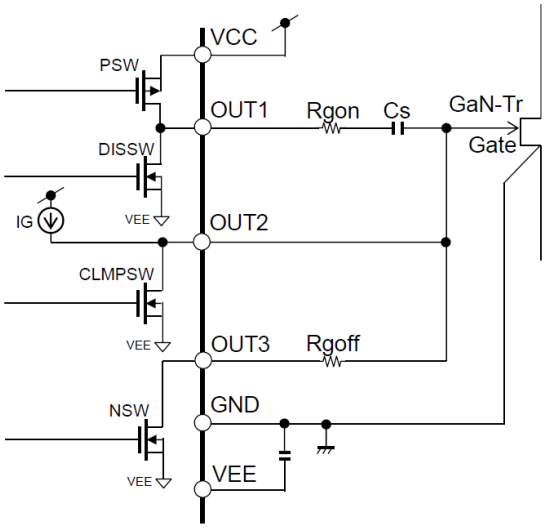


Figure 2.4. Functional block diagram of Panasonic x-GaN gate driver IC [21].

While this gate driver has several advantages in the easily tunable negative off-state gate voltage and steady-state gate current, manufacturers verify that a standard MOSFET driver is suitable for driving the GaN GIT in that it requires only a few milliamps of steady-state gate current to drive [10]. In Chapter 3, it will be shown that at least 10 mA steady-state current is recommended for driving the devices, as the on-resistance is also a function of gate current and gate drive loss is a small portion of overall loss in this design.

2.2 Characterization and challenges

Characterization is an important aspect in the study of the steady-state and switching behavior of semiconductor devices, particularly wide bandgap devices that are in a less mature stage and in which the data sheet may be unavailable and less accurate for power loss models. For similar reasons, characterization helps in determining maximum operating conditions of the device when datasheets are unavailable or less mature. Characterization and modeling of power devices have been well covered in literature for Si and SiC devices [22-30]. Dynamic characterization, test setup, and measurement strategies for double pulse test (DPT) for Si and SiC are discussed in detail in [26], [27]. The concern in studying dynamic performance for wide bandgap devices, like SiC and especially GaN, is the fast switching behavior, which requires high bandwidth probes and careful PCB layout. Even poor layout of the measurement circuit can result in inaccurate results. Therefore, an updated methodology is presented for fast switching devices in [25] and [31-39].

Dynamic characterization is also useful for studying the limiting factors in utilizing wide bandgap devices. In [40], several factors are presented as limiting the switching speed

of GaN and thus limiting the utilization of these devices for maximum performance. Some of these limiting factors are turn-on and turn-off gate driver resistance, rise and fall time of gate driver output voltage, and fast switching-induced cross-talk. Another limiting factor in achieving fast switching is the presence of device and PCB parasitics [41]. Dynamic characterization allows for models to be developed that represent device behavior when these parasitics are present, such as parasitic inductance and device and PCB capacitance.

In [42, 43], the impact of various parasitic elements on overshoot voltage and cross-talk are studied and used to develop a model for SiC MOSFETs. Similar studies are required to understand the impact of these elements on GaN devices as well, since the faster switching of GaN may introduce more complications. Additionally, because the GIT gate drive includes a series capacitance in the gate loop, the interaction of different parasitic elements on switching behavior may differ from that of Si or SiC MOSFETs. Such a study was conducted in [41] on low voltage GaN FETs and reveals how the presence of PCB parasitics can have a significant impact on converter efficiency. By optimizing the layout, efficiency can be improved by up to 40%. Additionally, a loss analysis for the GIT specifically is presented in [44], which includes the C_s capacitor in the gate drive. However, while the impact of the parasitics is studied experimentally, they are not included in the model to correct for the discrepancies. In [45-48], static and dynamic characterization results for 600/650 V GaN HEMTs are presented in addition to models utilizing these results, such as *dv/dt*, cross-talk, and temperature dependent turn-on loss analysis. However, these same models are needed for the GIT specifically. Methodology for gate

drive and thermal design are also suggested for maximizing the voltage and current capability of a 600 V/30 A GaN GIT [49].

Besides dynamic characterization, static characterization is also necessary to accurately model device behavior during steady-state operation. In [50] and [51], the significance of difference static curves are presented for MOSFETs, and manufacturers of static characterization equipment have discussed how to use such equipment for key static tests, especially for wide bandgap devices. Static characterization results for the GIT in particular can reveal the trade-off between steady-state gate current and gate drive loss, which has not been presented.

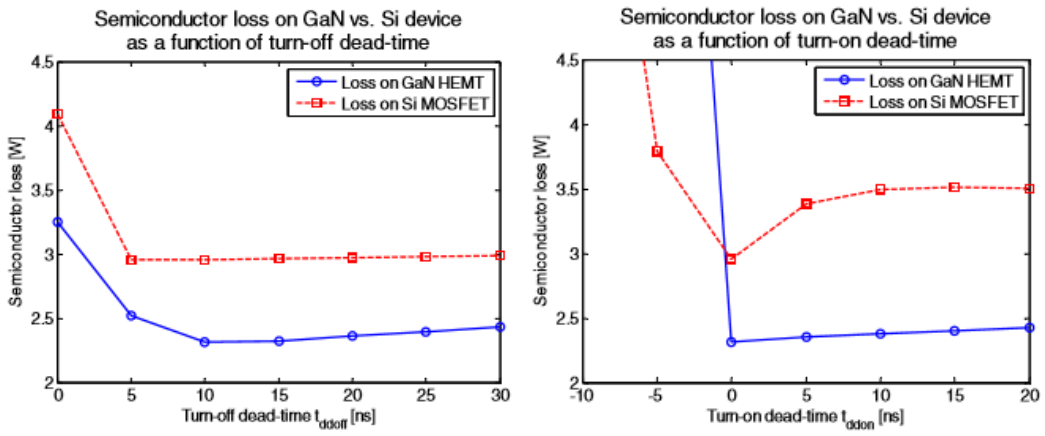
2.3 Dead time loss modeling and optimization

Considering a single phase leg in a voltage source converter (VSC), two devices are switched synchronously at a given frequency by a Pulse Width Modulated (PWM) signal in order to control flow of power. However, due to the non-ideal behavior of these devices, turn-off time is not instantaneous. Because of the finite amount of time it takes for the device to turn off, it is common practice to introduce a certain amount of time between the turn-on signals of each device. This timing synchronization, or dead time, prevents a shoot-through event, where the voltage source is shorted through both devices, and can cause increased power dissipation, degradation of the devices, and/or failure of the converter.

While dead time is necessary for safe operation of the converter, several adverse effects are introduced, such as voltage error, current distortion, and additional power loss. In addition, these adverse effects occur every switching cycle, meaning degradation of

inverter performance becomes more apparent at higher switching frequency. Therefore, while compensation and optimization techniques are well established for Si-based converters, existing approaches may be inadequate for devices that operate at higher switching frequencies, such as those based on GaN HEMTs. This knowledge gap is amplified by the trend towards more modern and versatile devices: as operating requirements (e.g., temperature, size, power rating) enforce new constraints on device design (e.g., power density, frequency), faster switching devices are developed, such as GaN. Therefore, updated dead time loss evaluation of these new devices, like the GIT, are becoming increasingly important along with updated optimization techniques.

The impact of dead time has been studied extensively for Si and SiC devices and has recently been of interest for GaN devices, since the loss mechanism for GaN during the dead time differs from that of a MOSFET body-diode. MOSFETs have an intrinsic diode that consists of a p-n junction, which is responsible for conducting the reverse current during dead time. Because of the presence of this intrinsic diode, reverse recovery loss will be induced. The GaN GIT, however, is a lateral device that consists of no parasitic diode but does have the capability of conducting reverse current. This is often termed a majority carrier body diode, or "diode like behavior [46]," and will result in no reverse recovery loss. In Figure 2.5 it was shown that 100 GaN HEMTs revealed lower loss for all dead times from zero to 20 ns compared to similar rated Si MOSFETs, with the exception of negative dead times [52].



(a) (b)

Figure 2.5. Loss comparison on power devices as a function of (a) turn-off dead time t_{ddoff} (b) turn-on dead time t_{ddon} [52].

The reason for higher loss during negative dead time is that the much faster switching speed of GaN provides a low-resistance, short circuit path, much lower than that of Si [52]. From zero to -5 ns, the loss in GaN increases to 8.85 W compared to the 0.83 W increase in the Si device. Above zero, although the power loss in GaN is lower than Si, the loss begins to increase at a faster rate than the Si MOSFET because of the higher reverse voltage drop. This is because the reverse voltage drop in a lateral device is a function of negative gate voltage according to (2.1). The necessity of the negative gate voltage to mitigate cross-talk further adds to the importance of optimizing the design for low dead time loss in the lateral GaN device.

$$V_{sd} = V_{gd} - V_{gs} - IR_{dson} \tag{2.1}$$

An antiparallel SiC Shottky diode could eliminate the high reverse conduction loss [53], but this diode would add extra stray capacitance that would slow the commutation time and would prevent taking full advantage of the fast-switching speed of GaN and would

complicate the overall gate drive design [54]. Therefore, optimization of the dead time is essential for maximized efficiency in high-frequency, GaN-based converters. The simplest method of dead time selection is to set a fixed dead time for both turn-on and turn-off delays. While simple implementation is convenient, a fixed dead time is not as efficient as dynamic control and may not be suitable for some high-frequency GaN applications [55]. In order to determine if adaptive dead time control is necessary for the 4.5 kW inverter presented in this thesis, the impact of dead time loss on total converter loss is characterized and evaluated.

Analytical models have been developed to optimize dead time loss by achieving ZVS, at which point the dead time loss will equal zero. In [53, 56], models were developed for e-mode GaN HEMTS that model the turn-off time of the device and the optimal dead time for each switching transient. Using this type of model, the dead time can be adjusted every switching cycle to achieve ZVS and eliminate the loss. However, the dead time loss itself is not modeled and the impact of dead time loss without adaptive scheme is not evaluated. Additionally, these models are based on conventional voltage driven devices and do not consider the series capacitance introduced in the GIT gate driver. In [52, 57], the impact of dead time and dead time loss itself is evaluated for DC-DC converters. However, in AC-DC operation, the dead time loss mechanism changes depending on the instantaneous current in the line cycle, so the average loss depends on RMS current, DC bus voltage, and temperature, which are not considered in the literature. This loss also depends on gate drive design, device parameters, and device/PCB parasitics, so the models are not relevant for a different gate drive design like that for the GIT.

2.4 Short circuit robustness and protection schemes for GaN

The requirement of fast overcurrent and short-circuit protection for WBG devices has been shown to be much stricter than conventional Si devices. Compared to Si, the drift region of GaN devices are designed to take advantage of the high electric field breakdown of GaN material, and therefore, a much higher electric field is to be expected when high drain voltage is applied, leading to higher power dissipation density than Si [6]. Likewise, high short-circuit current is more likely to concentrate in the AlGaN/GaN interface rather than the bulk material of a vertical device, causing extreme localized temperature rise. The higher saturation velocity of GaN also results in higher saturation current, further increasing the likelihood of localized temperature surge during short-circuit event and consequently lower robustness [58]. Therefore compared to Si or SiC MOSFETs, GaN has been shown to exhibit a much shorter short-circuit withstand under high bus voltages [59, 60]. For example, a 600 V GaN FET can be destroyed during a short circuit event in as little as 400-600 ns at 400 V [61-69], and in some cases as low as 200 ns [70-72]. However, studies show that the GaN HEMT can be quite robust at lower bus voltage, sustaining short-circuit for 10 µs for V_{bus} < 300 V, which passes traditional Si standards [73]. Specific to the GIT, the maximum drain current can be limited by I_g during turn-on, and correlation between short-circuit withstand time and gate current was observed in [74], although no correlation was observed in [75].

A common protection scheme for most power devices is desaturation protection, shown in Figure 2.6 [60]. Desaturation protection requires sensing of the drain-source voltage, and triggers the gate driver to turn off when this voltage indicates that the device

has entered the saturation region. This scheme is limited for several reasons. First, a sensing diode must be used to protect the sensing circuit from the high drain-source voltage when the device is off. This means a blanking time at least as long as the voltage fall-time is required, which reduces the response time and adds capacitive loading to the output capacitance of the device. Additionally, the overcurrent threshold is set by the saturation current at the gate driver voltage, which is a strong function of junction temperature. Therefore, a much higher overcurrent threshold must be chosen to account for worst case condition at maximum operating junction temperature.

Desaturation overcurrent protection has been shown to protect GaN devices in as short as 200 ns [76-78]; however, the parasitic capacitance of sensing diode, D_{ss}, adds to the output capacitance, C_{oss}, of the GaN device, which may increase both response time of protection and the switching loss during normal operation. A unique gate-sensing short-circuit protection scheme was developed for the GIT, which resulted in a protection time of < 200 ns [17]. Unlike desaturation protection, the circuit shown in Figure 2.7 adds no capacitive loading to the drain of the GIT, but the sensing circuit does load the C_{gs} of the device. Therefore, this thesis will compare the performance of the gate-sensing scheme to desaturation protection in regards to induced switching loss and future work will focus on comparing protection performance. Other protection schemes include the use of a shunt resistor and current transformer, which add to the power loop inductance. Therefore this work will focus on a comparison to desaturation.

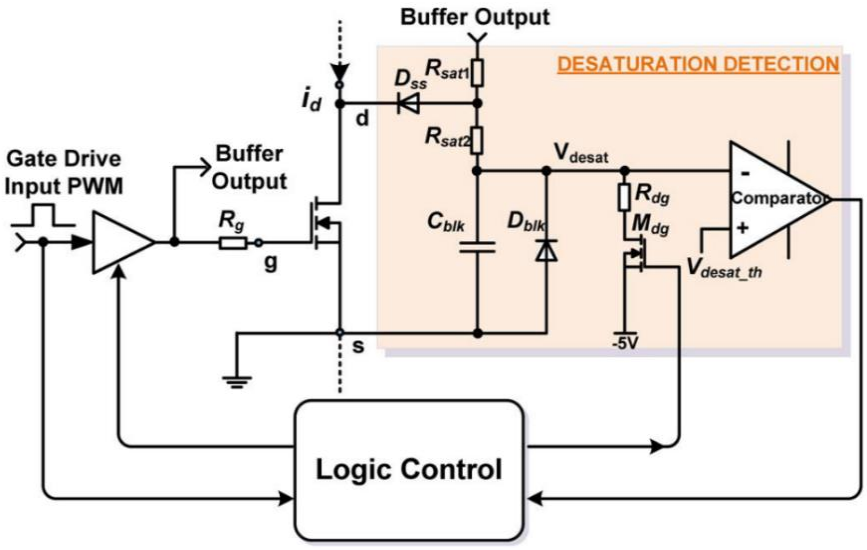


Figure 2.6. Schematic of a desaturation overcurrent protection scheme [60].

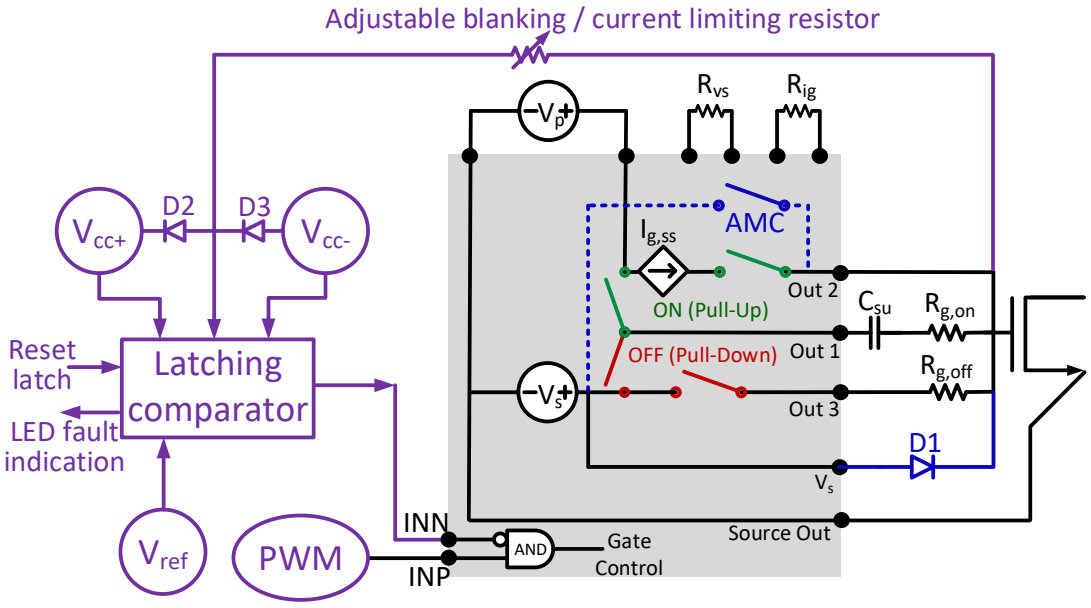


Figure 2.7. Functional block diagram of gate-sensing protection circuit, with the gate driver IC (AN34092B) functions enclosed in the grey box [17].

Chapter 3

GaN GIT Characterization and Design Considerations

3.1 Introduction

Due to a lack of datasheet information and the early stages of device manufacturing, the design of a GaN-based converter required a comprehensive characterization of both the static and dynamic behavior of the selected 600 V/30 A gate injection transistor (GIT). Additionally, a thorough characterization of the device behavior is necessary for future development of device switching loss and overshoot models incorporating the impact of the additional gate drive parameters for the GIT gate drive scheme. The first converter was designed utilizing this device in a TO-leadless (TOLL) bottom-cooled package, whereas the second converter was designed utilizing the same device in a top-cooled, DSO-20-85, 20-pin package for improved thermal design and PCB power stage layout. The data collected from these tests were used for modeling conduction and switching loss and for understanding how the behavior of the devices under steady-state and transient operation will impact the overall performance of the converter. The impact of package and PCB layout parasitics on the bottom-cooled and top-cooled designs is studied.

3.2 Static characterization

Static tests were conducted using the Keysight B1505A curve tracer, which includes the ultra-high current expander (I-V test fixture) and capacitance test fixtures. The block diagram in Figure 3.1 describes the overall setup of the static tests at room temperature, with an example of the default TO-220 test fixtures. For the purposes of these tests, a dedicated PCB was designed to replace the default TO-220 test fixture, shown in

Figure 3.2. All high temperature static tests were conducted in an oven to ensure the junction temperature of the device is accurately controlled and for calibrating hot plate temperature based on R_{dson} measurement. The longer cables necessary to reach the devices in the oven were thick enough to ensure that parasitic resistance did not significantly affect the on-resistance measurement. Room temperature results in the oven were compared with original room temperature results to verify that the setup had no impact on on-resistance measurements.

3.2.1 Steady-state current selection

Unlike a conventional voltage driven device, the GIT requires a constant gate current to maintain the forward bias voltage of the gate diode in steady-state operation,

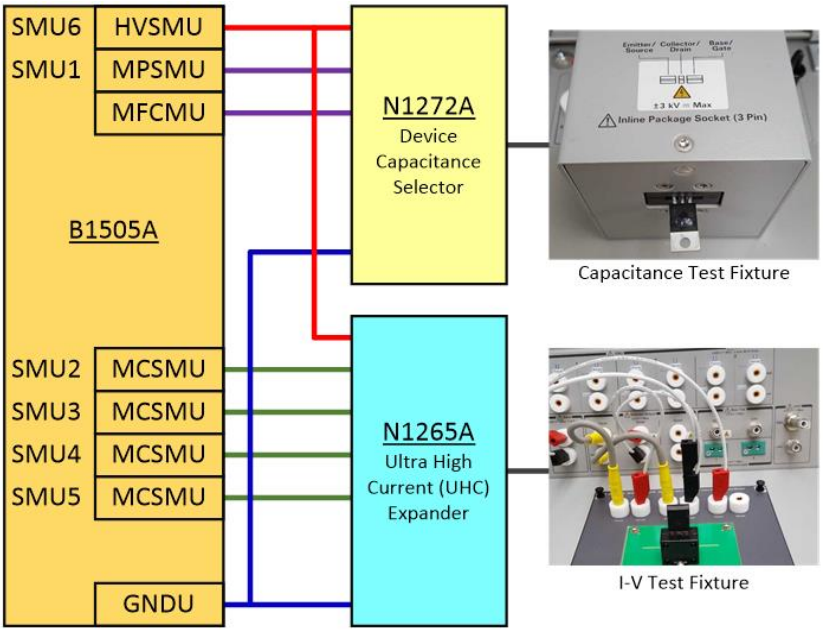
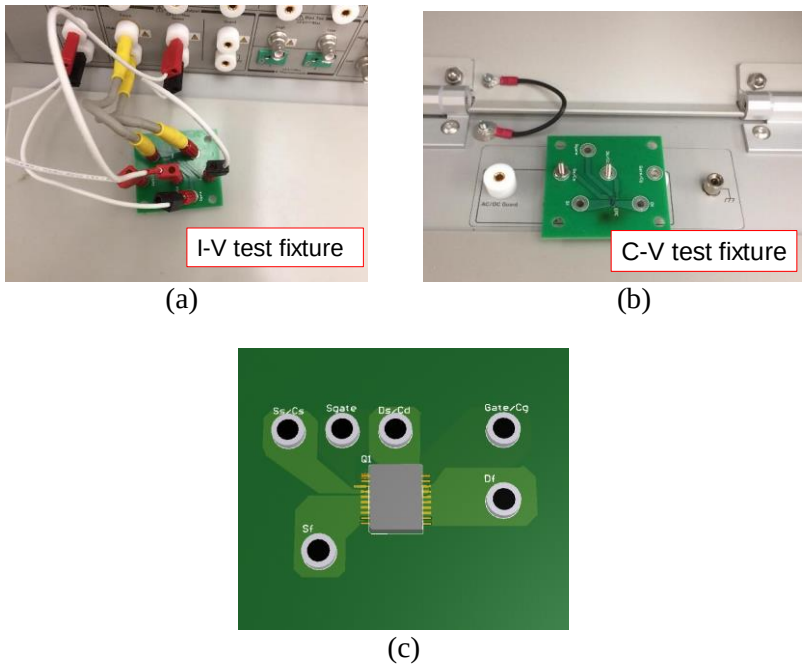


Figure 3.1. Function block diagram of Keysight B1505A curve tracer.



(a) (b)

(c)

Figure 3.2. (a) I-V test fixture, (b) C-V test fixture with DSO package, and (c) top view of PCB static test board.

which is typically around 3.5 V depending on the steady-state current. To determine the amount of gate current necessary to enhance the channel, the following characteristics are needed: gate current vs. gate voltage, on resistance vs. gate current, and internal gate resistance. The gate current vs. gate voltage characteristic is very similar to a traditional diode characteristic in which the voltage across the diode depends on the forward bias current. Because the gate voltage of the GIT determines the on-resistance of the channel, it is more accurate to plot the on-resistance vs. gate current as opposed to the gate voltage vs. on-resistance. Finally, the internal resistance of the gate induces power loss, so while on-resistance decreases with higher gate current, gate loss will also increase. Therefore, both should be taken into consideration when designing the gate drive current. Additionally, while the GIT has no maximum gate voltage, there is typically a maximum

allowable gate current in the tens of milliamps range during steady-state, and to avoid degradation or failure, this current should not be exceeded. For the device under test (DUT), the maximum constant gate current should not exceed 50 mA, while the maximum pulsed current should not exceed 2 A.

Static characterization was conducted on several devices to measure the variation of on-resistance vs. gate voltage and gate current. The differences between these two trends are shown in Figure 3.4 and Figure 3.5. In Figure 3.4, the on-resistance reaches a nominal room-temperature value of 55 Ω at V_{gs} = 3.4 V. Results in Figure 3.3 show that the corresponding gate current at V_{gs} = 3.4 V is ~20 mA. This is verified in Figure 3.5, where the on-resistance reaches the nominal value at around i_g = 20 mA. This is further verified in Figure 3.6, a plot with $R_{ds,on}$ normalized around 50 mA gate current. From this plot, a gate current ≥ 2 mA is adequate to forward bias the gate diode. However, a gate current ≥ 10 mA is recommended to achieve low on-resistance while remaining below the maximum gate current and minimizing gate drive loss. For this design, a steady-state gate current of 20 mA was chosen to achieve the nominal 55 mΩ on-resistance for the entire junction temperature operating range. Figure 3.7 also shows the impact of I_{gss} and turn-on gate drive speed on gate drive loss and R_{dson}. Considering the gate leakage current of an insulated gate GaN device results in a gate drive loss of ~0.005 W at 140 kHz switching frequency [11], the gate drive loss for the GIT is an order of magnitude higher, though still an insignificant portion of overall converter loss in this design.

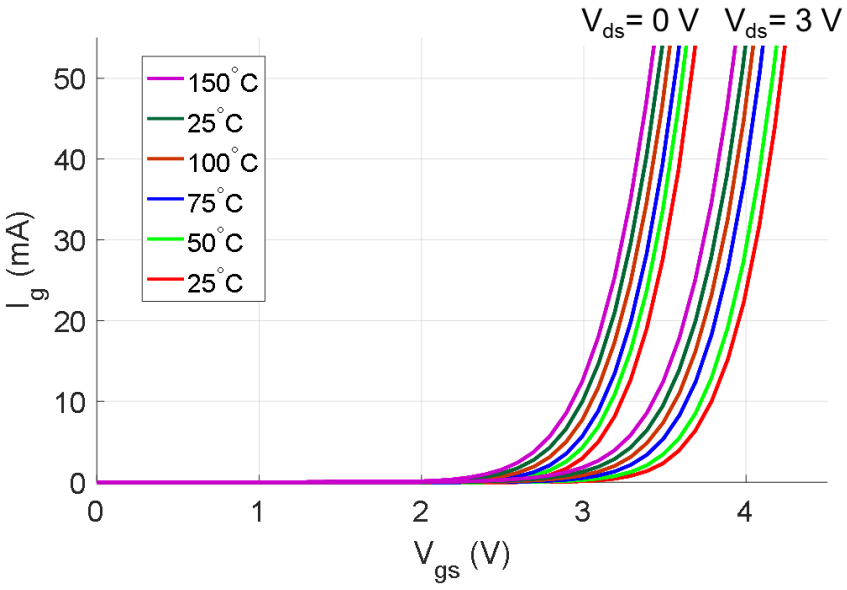


Figure 3.3. Gate current (I_g-V_{gs}) vs. temperature for V_{ds} = 0 V and 3 V.

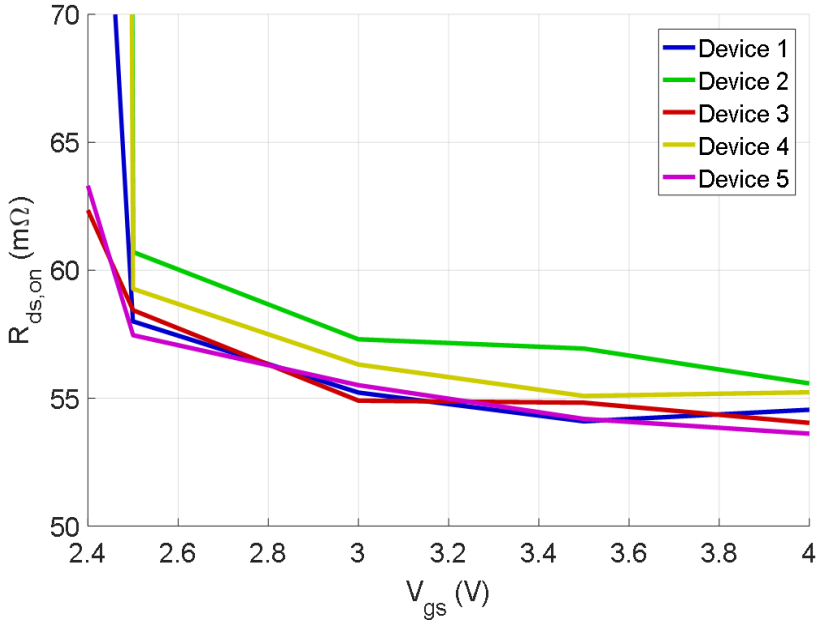


Figure 3.4. On-resistance vs. gate voltage for five samples with I_d = 8 A. Datasheet value of $R_{ds,on}$ = 55 mΩ to 70 mΩ at room temperature.

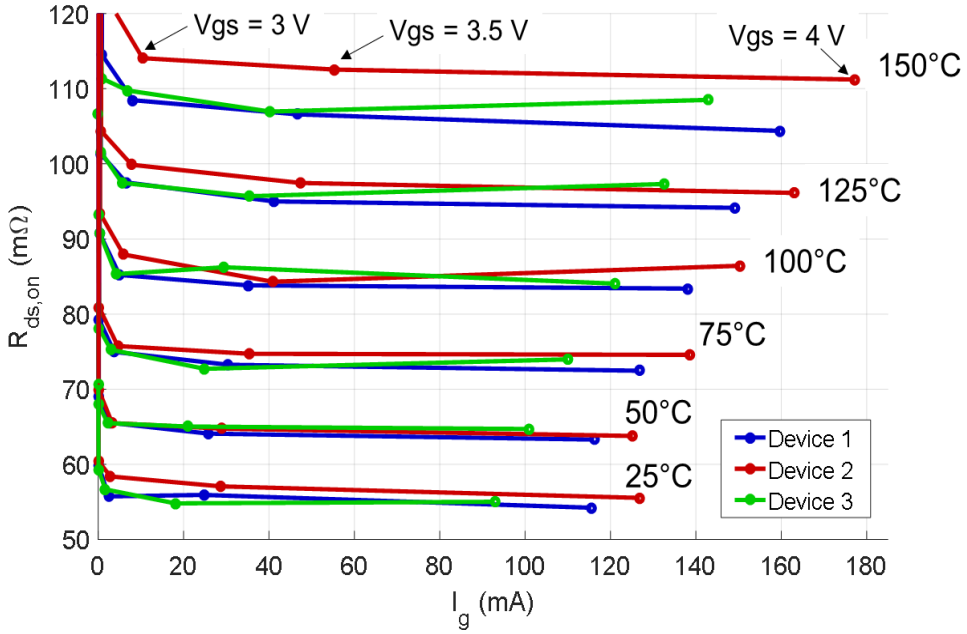


Figure 3.5. $R_{ds,on}$ vs. gate current and junction temperature for 3 samples at I_d = 8 A.

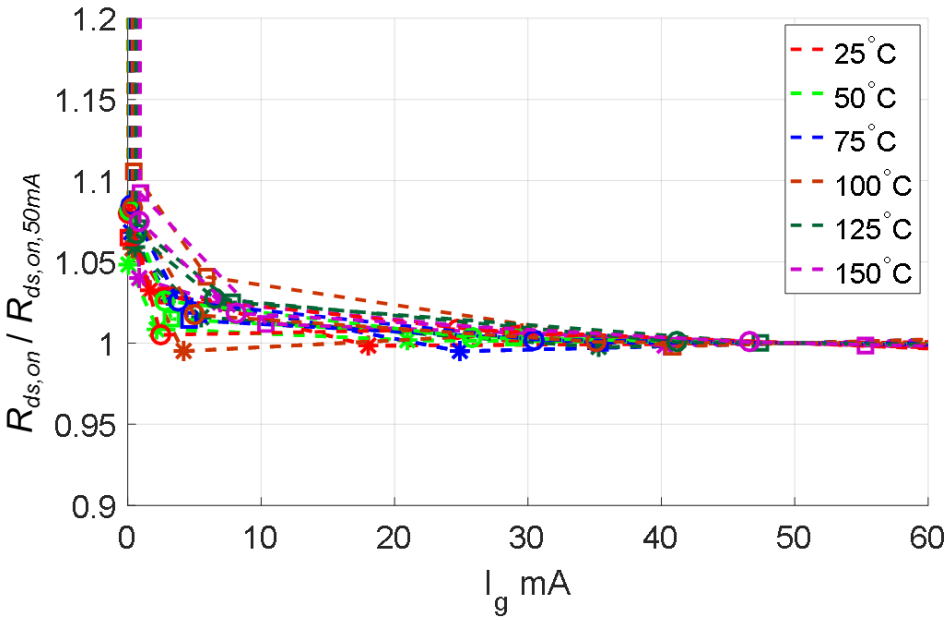


Figure 3.6. Normalized $R_{ds,on}$ vs. gate current and temperature for gate drive design consideration, normalized to the I_g = 50 mA point.

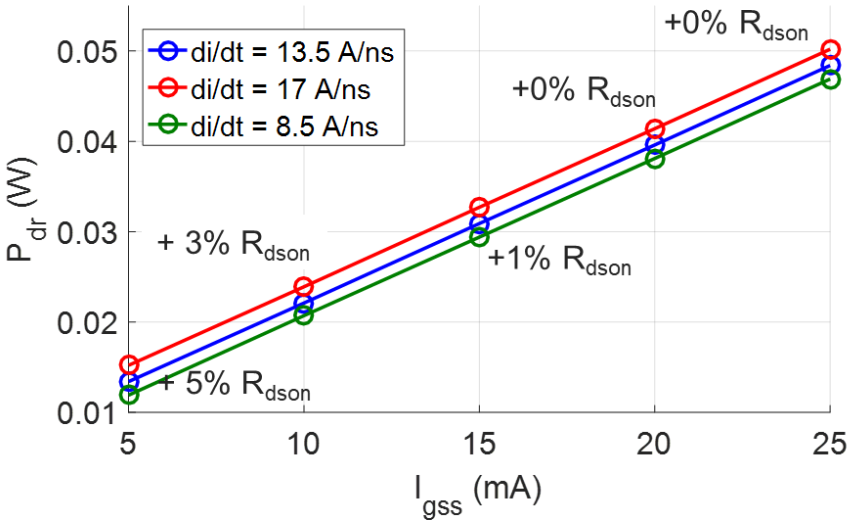


Figure 3.7. Gate drive loss vs. I_{gss} and turn-on di/dt for f_{sw} = 140 kHz.

3.3 Dynamic characterization

Dynamic characterization was performed on the GaN GITs to measure voltage and current waveforms during hard turn-on and turn-off transients using the conventional double pulse test (DPT) as shown in Figure 3.8. With this data, the switching loss, turn-on/turn-off times, and voltage overshoot can be measured for use in the overall converter design and future modeling. Additionally, this process provides the opportunity to optimize and adjust the gate drive circuit parameters and verify in the overall power stage design. In the majority of tests, the synchronous (or upper) device remained "off" in order to operate similarly as a free-wheeling diode to allow the load current ample time to commutate. In this way, the turn-off time for various operating conditions was measured, and other parameters, such as dead time setting, were designed.

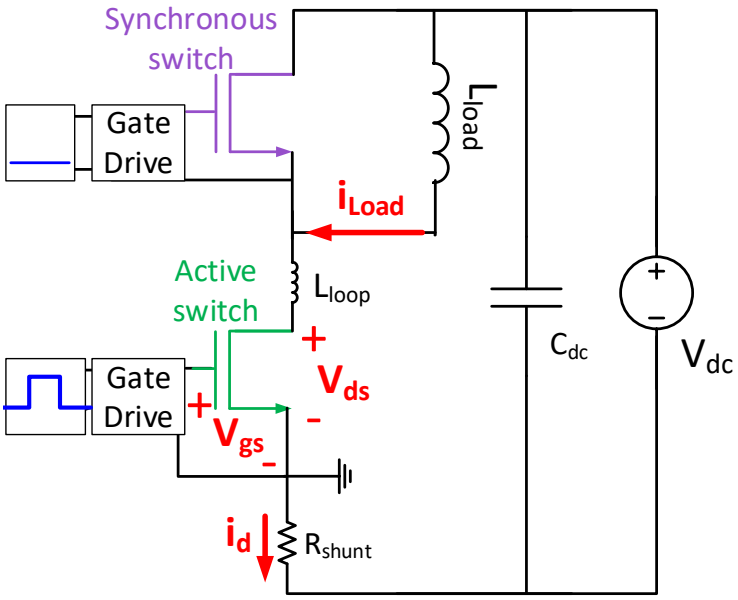


Figure 3.8. Double Pulse Test (DPT) circuit used for dynamic characterization.

3.3.1 Consideration of device packaging

Device packaging is of particular interest especially in the design of high-frequency devices like GaN. This is because the fast switching capability of the device makes switching behavior very sensitive to parasitic inductance and capacitance. To allow for faster switching with low overshoot voltage, a package with low parasitic inductance is desirable. In Phase 1 of the 4.5 kW inverter design, a bottom-cooled package of the 600 V/70 mΩ device was utilized, and in Phase 2, the top-cooled version of the same 600 V/70 mΩ device was used. While the parasitics of the device package itself are important, the parasitics of the power loop may play a larger role in improving overall performance depending on the location of the device thermal pad. The overall parasitics of the design for both devices are compared in Table 3.1. It can be seen that although the overall package

parasitics of the bottom-cooled device are lower, the overall power loop parastics are lower when utilizing the top-cooled package. This is because the thermal pad is on the top-side of the device, meaning the heat sink does not need to connect to the device through thermal vias, and a vertical power loop layout is possible. For Phase 1 design, a lateral power loop was required due to the bottom-side thermal pad. This resulted in a power loop inductance of ~13 nH with the DPT shunt resistor in the power loop and 10 nH without. For Phase 2, the top-side thermal pad allowed a vertical power loop design, meaning the loop area is reduced and the magnetic flux is cancelled by using the inner layer of the PCB as the current return path. This resulted in a reduction in power loop inductance to 6 nH with the shunt resistor in the power loop and 4 nH without.

This power loop inductance value was estimated through a post-processing method in Matlab as discussed in [45]. The loop inductance is estimated based on the voltage drop during turn-on shown in Figure 3.9. After processing the *di/dt* during the turn-on transient, the loop inductance can be adjusted until the red curve, $L_{loop} \cdot di/dt$, is equal to the voltage drop in V_{ds} due to loop inductance. This method also helps determine the appropriate

Table 3.1. Comparison of device and layout parasitics of bottom-cooled and top-cooled 600 V devices.

Device package	Layout	L_{loop} (nH)	L_{ds} (nH)	L_g (nH)	L_s (nH)
Bottom-cooled	Lateral	10	0.92	3.93	0.54
Top-cooled	Vertical	4	2.1	5.44	1

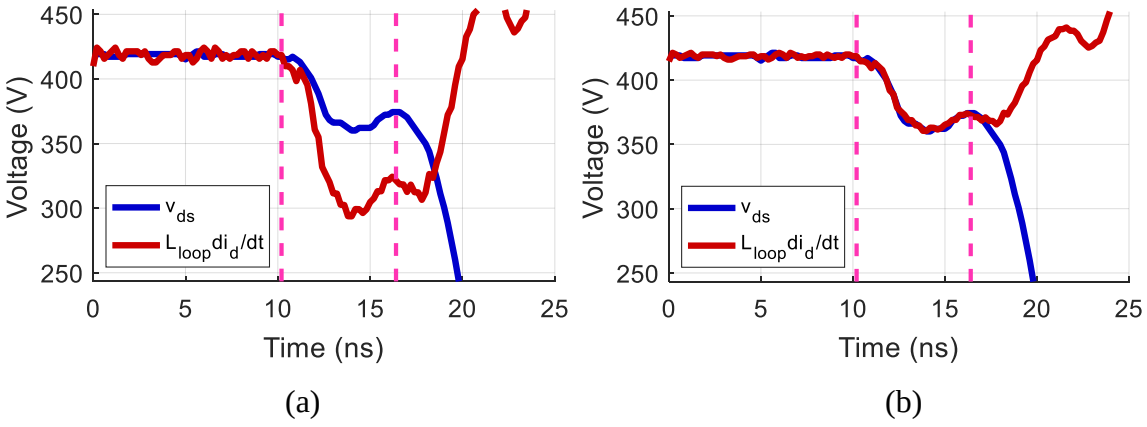


Figure 3.9. Estimation of Lloop using Matlab post-processing method, with an estimate of (a) 13 nH and correct estimate of (b) 6 nH.

deskew time for the drain current measurement.

Because of the significantly lower power loop inductance, the overall switching loss can be reduced by increasing the switching speed. This is due to the fact that the overshoot voltage on the synchronous device during a turn-on transient is dependent on max $di/dt \cdot L_{loop}$. This was verified by comparing the turn-on overshoot voltage of both the lateral and vertical power loop and is shown in Figure 3.10. With a *di/dt* of 12.5 A/ns, the overshoot voltage overall was reduced by 30-50 V by utilizing the top-cooled package and vertical power loop design. In Phase 1 converter using the bottom-cooled package device, the maximum overshoot voltage should not exceed the 600 V rating, limiting the di/dt to 12 A/ns. Because the loop inductance was decreased in Phase 2 by roughly half, there was margin to increase the *di/dt*. The reduction in switching loss in Phase 2 converter was mainly observed at higher load current, reducing the switching loss by 25% as shown in Figure 3.11.

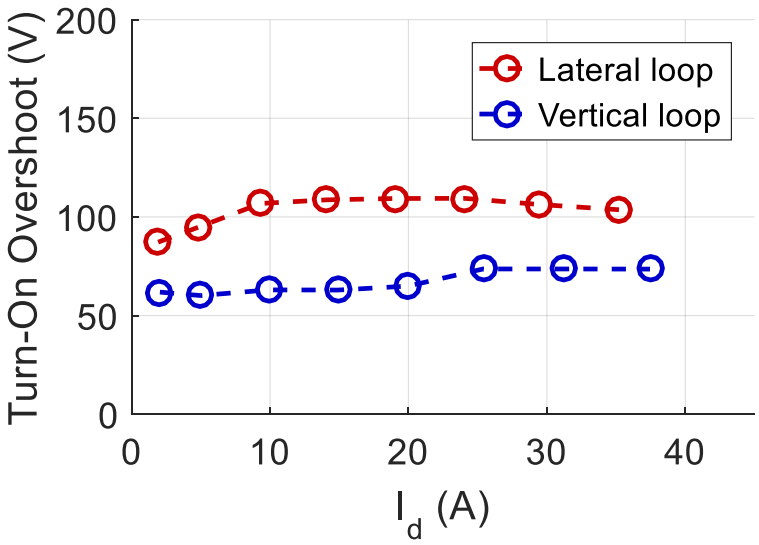


Figure 3.10. Impact of power loop inductance on turn-on overshoot voltage with di/dt = 12 A/ns and V_{dc} = 400 V.

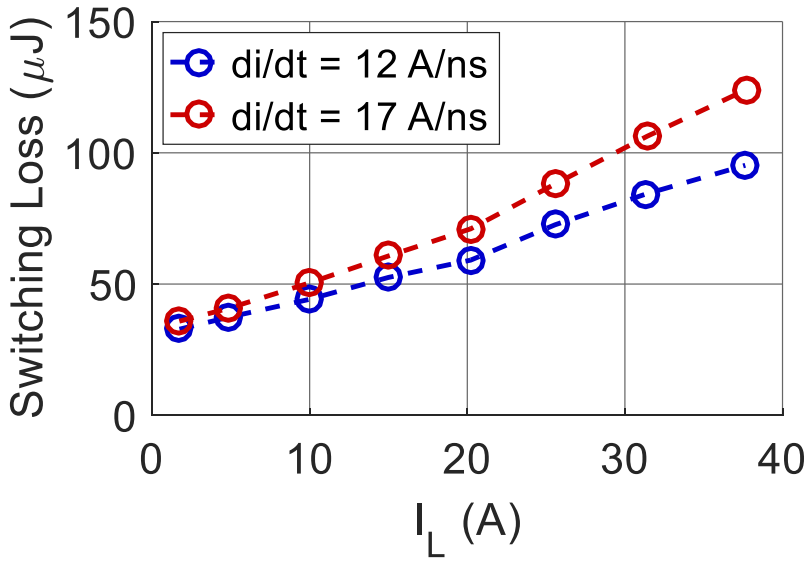


Figure 3.11. Reduction in switching loss due to increased di/dt margin with vertical power loop.

Despite the increase in *di/dt* margin, the measured switching loss induced in the top-cooled device was still higher than that of the bottom-cooled device. For the same *di/dt*, the measured turn-on switching loss was 40% higher in the top-cooled package than the bottom-cooled. A look back at Table 3.1 shows that the gate parasitics are 2 nH higher in the top-cooled device, and Figure 3.12 shows the cause of the higher switching loss. First, the lower L_{loop} results in a smaller voltage drop across the device, increasing loss during the first *di/dt* interval. During the C_{oss} discharging time, the voltage fall time also takes longer. Further testing revealed that by increasing the gate loop inductance, this behavior was made worse, further increasing switching loss. Therefore, a likely cause of increased loss in the top-cooled device is both lower L_{loop} and higher L_g.

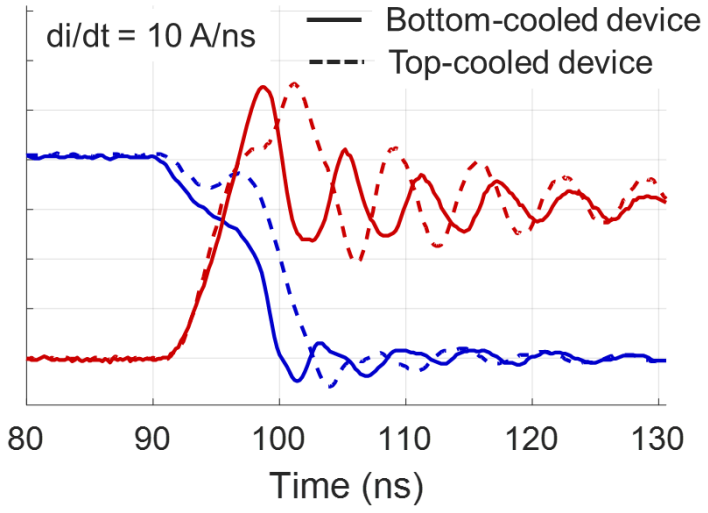


Figure 3.12. Comparison of turn-on waveforms of top-cooled and bottom-cooled GaN GIT.

3.3.2 Consideration of gate resistance

Unlike a conventional voltage driven gate driver, an optimal gate driver for the GIT should provide a dynamic pulse of gate current in the beginning of the switching transient to improve the switching loss. This means that the conventional models for switching behavior and loss are not applicable for this converter, and new characterization results must be obtained to develop new models for the GIT. The series RC network in the gate drive circuit impacts switching performance in two key ways: switching loss and voltage overshoot. The GIT in this study is rated for 600 V, so typically the operating voltage should not exceed ~450 volts to allow margin for transient voltage.

However, a study of the leakage current for this device vs. bus voltage and junction temperature shows that even at elevated junction temperature, the leakage current is acceptable up to ~700 V, shown in Figure 3.13. Based on manufacturer recommendation to limit leakage current to 250 μJ, an allowable transient voltage of 650 V was determined acceptable for this application. Likewise, the maximum DC bus voltage allowed in the converter depends on the overshoot voltage, and because the conventional methods of reducing overshoot voltage are to reduce switching speed and/or PCB power loop parasitics, this section seeks to find a trade-off in switching speed and overshoot voltage reduction in this unique capacitive gate drive scheme for the GIT.

The methodology for this study involved sweeping the gate drive parameters, C_{su} and V_{dr}, with a 300-500 V bus voltage and up to 40 A load current. The turn-off resistance remained zero ohms due to the negative impact on turn-off switching loss and overshoot

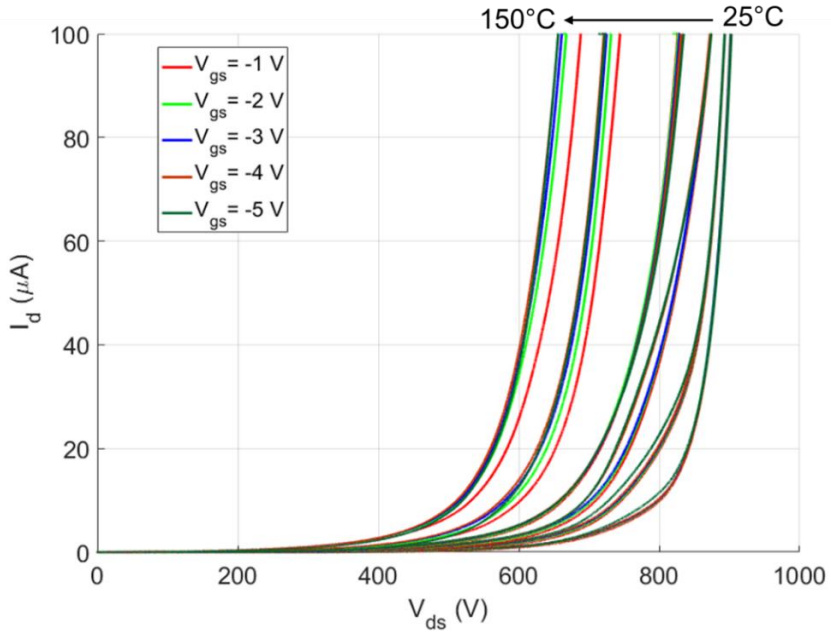


Figure 3.13. Leakage current characteristic of 600 V device with increasing negative gate voltages and temperature.

voltage. This can be seen in Figure 3.14 where the turn-off resistor was swept from 0-20 Ω. Intuitively, a slower turn-off speed should decrease the overshoot voltage. However, this trend reveals that the overshoot voltage actually increases as the turn-off resistance is increased. Up to 15 A, there is a negligible difference in overshoot magnitude, although it is generally lower with higher resistance. For load current greater than 15 A, the trend becomes more linear as R_{off} is increased, eliminating the beneficial dip that occurs after ~20 A with R_{off} = 0 Ω. One explanation for this phenomenon is the gate driver turn-off mechanism.

The Panasonic gate driver has three outputs as discussed in Chapter 2. However, a ~45 ns delay between the closing of Out 1 and Out 3 was observed during testing. The original gate driver circuit is shown in Figure 3.15 (a). This delay results in the turn-off

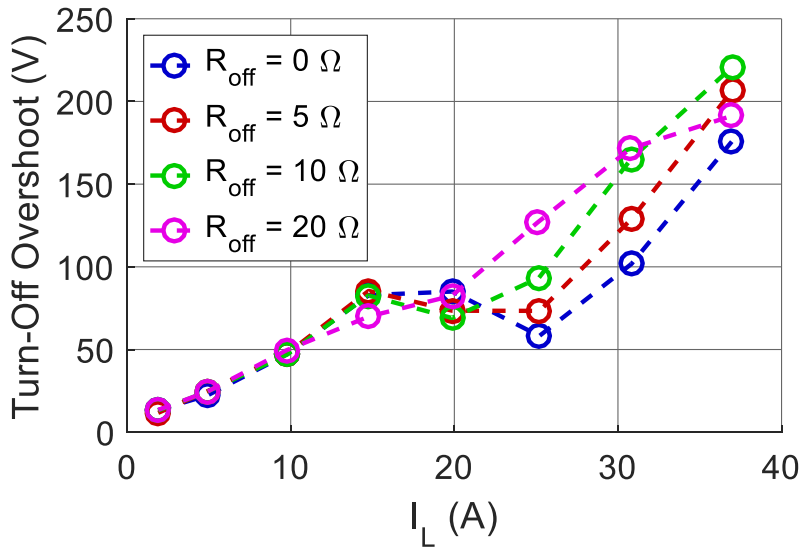
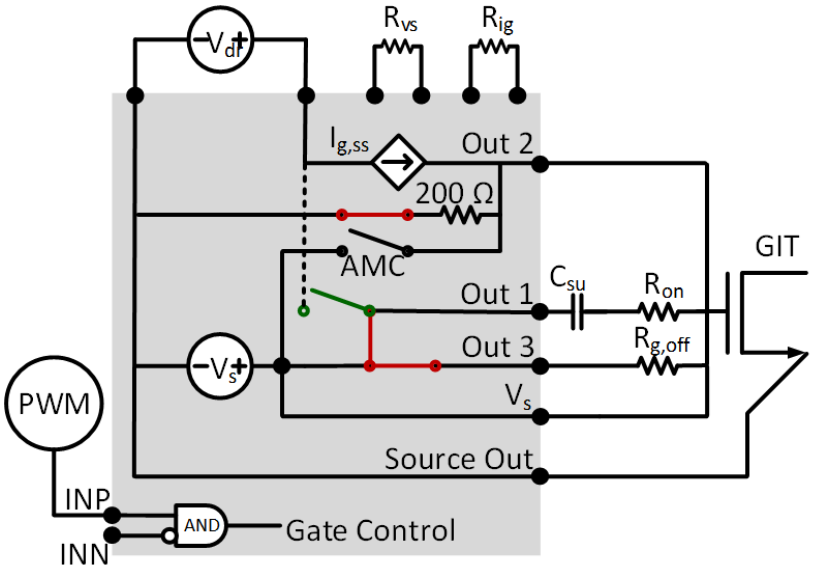
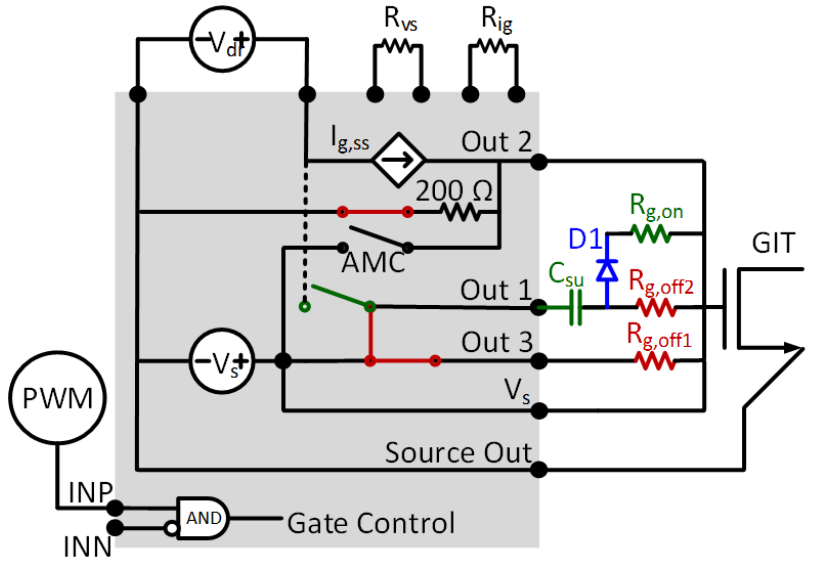


Figure 3.14. Impact of Roff on turn-off overshoot voltage with Vdc = 400 V.

gate current to flow initially through the lower resistance C_{su} path. By the end of the delay, the turn-off transient is nearly over, and the turn-off resistor has little to no impact. To overcome this delay, a diode, *D1*, and turn-on resistor, R_{on}, were inserted between C_{su} and the gate of the GIT, shown in Figure 3.15 (b). This allows a much larger resistor, R_{goff2}, be used for the initial turn-off of Out 1 to slow the turn-off speed without affecting the turn-on speed. The overshoot voltage observed from subsequent testing reveals a similar phenomenon without the *D1* diode, meaning the impact of the gate driver is only a partial explanation for the higher overshoot voltage with slower switching. In fact, no beneficial reduction in overshoot voltage was observed until $R_{g,off1}$ and $R_{g,off2}$ were increased to 100 Ω and 1 kΩ respectively, shown in Figure 3.16. However, the benefit is negligible due to the significant increase in turn-off speed, shown in Figure 3.17. Therefore, for this design, the original circuit in Figure 3.15 (a) was used with $R_{g,off}$ = 0 Ω and R_{on} = 10 Ω.



(a)



(b)

Figure 3.15. (a) Original circuit diagram of Panasonic x-GaN gate driver compared to (b) circuit with an additional diode and resistor connected externally to Out 1.

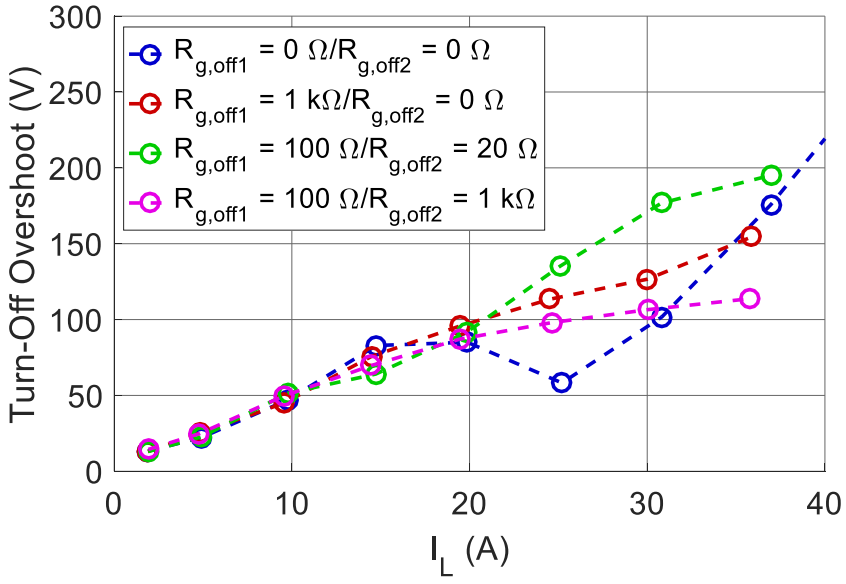


Figure 3.16. Impact of D1 and additional turn-off resistance on turn-off overshoot voltage for V_{dc} = 400 V.

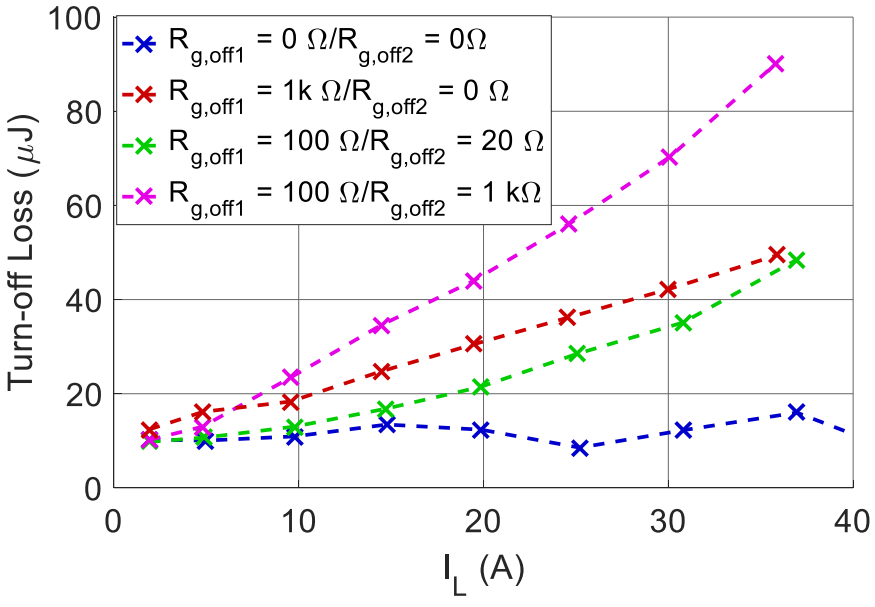


Figure 3.17. Impact of D1 and turn-off resistance on turn-off switching loss for V_{dc} = 400 V.

3.3.3 Overshoot voltage vs. switching loss tradeoff

With the value of $R_{g,off}$ determined, the next step is to tune C_{su} and V_{dr} to further study what is the optimal combination of gate drive parameters for overall lower voltage overshoot and switching loss. First, the series gate capacitor was swept from 0.5 nF to 1.5 nF with a fixed gate drive voltage. Second, the gate drive voltage was swept from 9 V to 12 V with a fixed C_{su}. The results in Figure 3.18 and Figure 3.19 indicate that the impact of C_{su} on switching speed with fixed V_{dr} is non-linear compared to the impact of V_{dr} with fixed C_{su}. Nonetheless, it is clear that higher gate drive voltage and higher series capacitance reduces the overall switching loss. There is also a design requirement to maintain a transient voltage below 650 V, and a higher gate drive voltage and speed-up capacitance may increase the turn-on overshoot voltage. Therefore, the turn-on overshoot voltage was measured for the same gate drive parameter sweep.

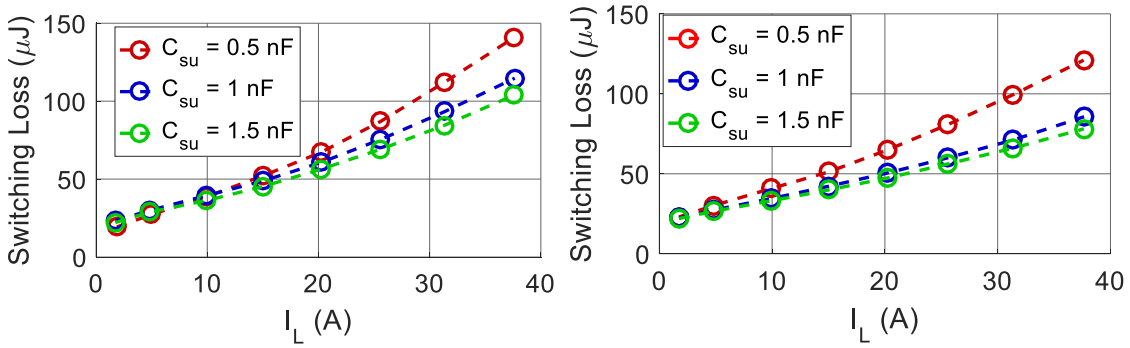
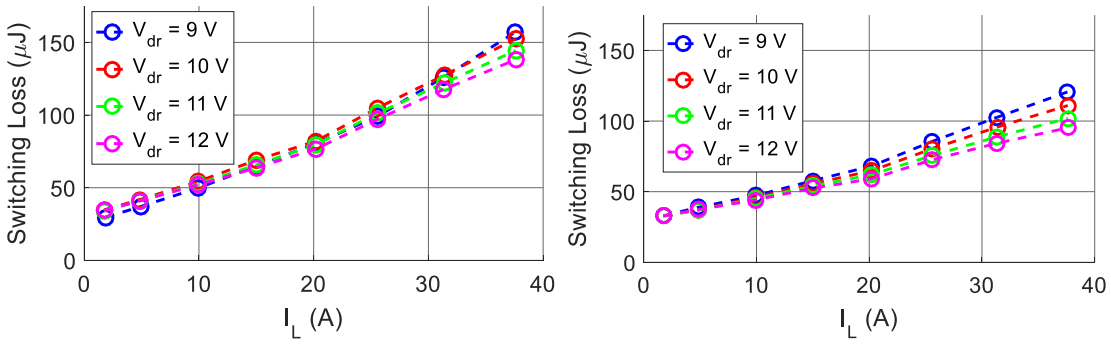


Figure 3.18. Impact of Csu on switching loss, (a) Vdr = 9 V and (b) Vdr = 11 V.



(a) (b)

Figure 3.19. Impact of V_{dr} on switching loss with (a) C_{su} = 0.5 nF and (b) C_{su} = 1.5 nF

The results in Figure 3.20 and Figure 3.21 show the impact of various gate drive parameter combinations on turn-on overshoot voltage. Again, the C_{su} sweep appears to have a non-linear trend compared to V_{dr}. Therefore, there may exist an optimal combination of C_{su} and V_{dr} that results in lowest switching loss and overshoot voltage. First, all combinations that were at the maximum overshoot boundary were selected. Finally, of these selections, the combination with the lowest switching loss was chosen as the design for the final converter. From the two 3-D plots in Figure 3.22, the optimal combination utilizing these devices is a combination of 12 V and 1.5 nF. Although this is the fastest combination tested, the overshoot voltage happens to be smaller than some slower combinations. In fact, beyond a particular *di/dt*, there appears to be negligible increase in overshoot voltage, though the switching loss continues to decrease. Because it was already determined that turn-off speed has little impact on the overshoot voltage, this study did not include the impact of gate drive voltage on turn-off overshoot voltage, as verified in Figure 3.23.

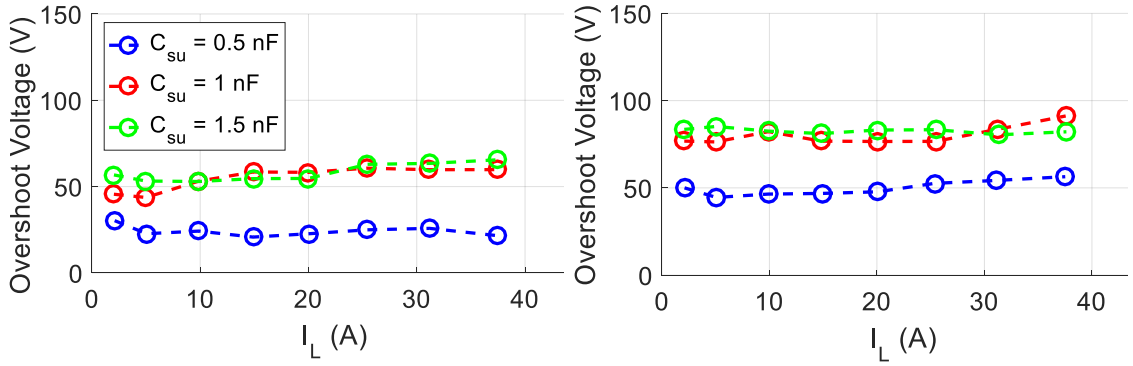


Figure 3.20. Impact of C_{su} on turn-on overshoot for (a) V_{dr} = 9 V and (b) V_{dr} = 12 V.

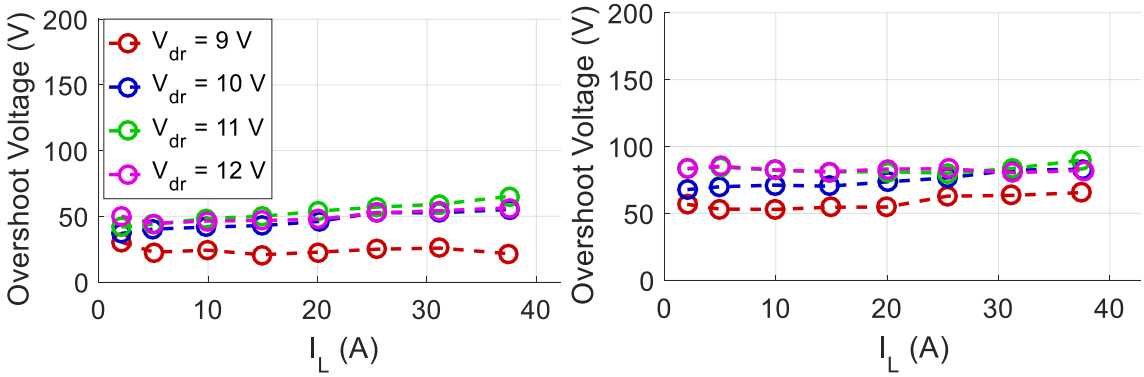


Figure 3.21. Impact of V_{dr} on turn-on overshoot voltage for (a) C_{su} = 0.5 nF and (b) 1.5 nF.

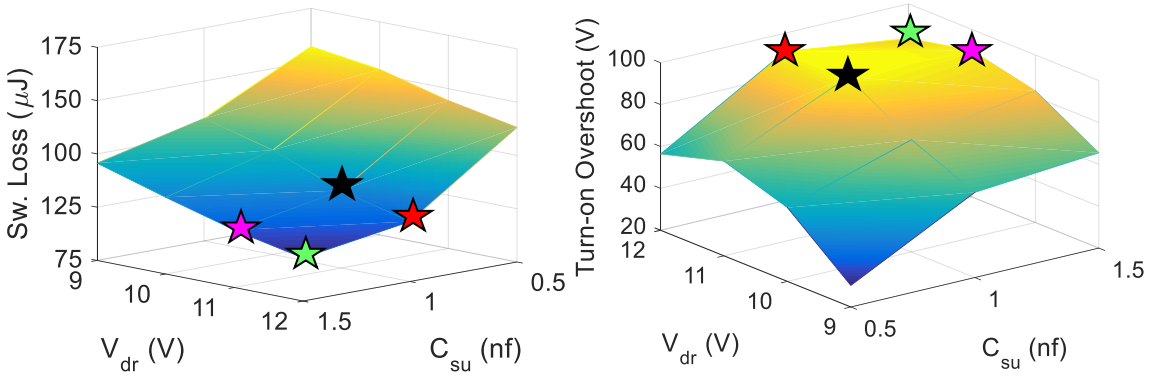


Figure 3.22. Switching loss vs. overshoot voltage trade-off for various driving voltages, V_{dr}, and series capacitance, C_{su} with V_{dc} = 400 V.

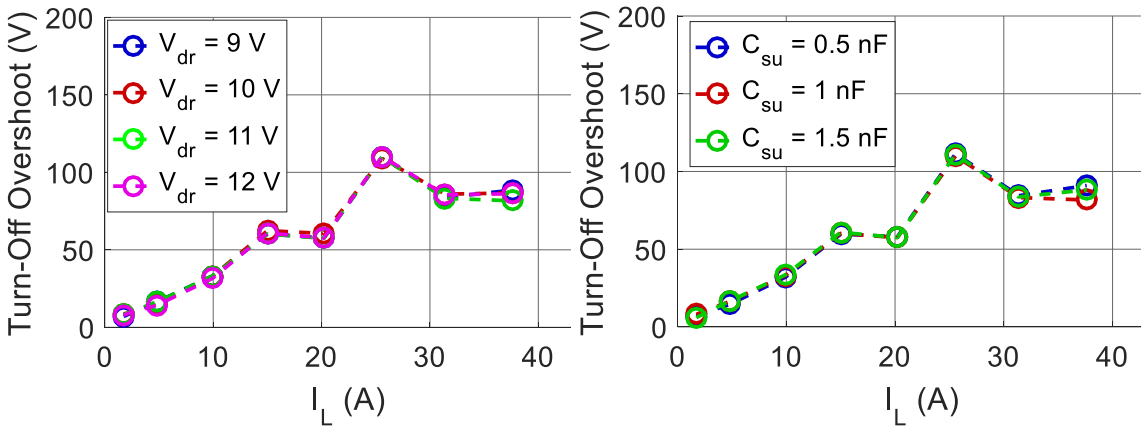


Figure 3.23. Impact of V_{dr} and C_{su} on turn-off overshoot voltage with V_{dc} = 400 V.

3.4 Overshoot voltage discrepancies

In Phase 1 converter testing, a discrepancy was observed between the overvoltage measurements characterized in the DPT and the measurements taken during continuous converter operation. An investigation was then conducted to determine the cause of the discrepancy. Several factors were taken into consideration, such as differences in power loop layout, measurement technique, and grounding configurations. Table 3.2 gives a summary of the differences observed between the DPT and converter test setups. In the initial investigation, the converter code was adjusted to perform a DPT on each phase leg of the converter. The overshoot measurements are shown in Figure 3.24, and a comparison is made between converter overshoot and DPT overshoot measurements. There is a clear difference in the trend between the converter testing and the original DPT. However, there is no difference between continuous operation and DPT operation on the converter overshoot measurements.

The original DPT was then conducted with the converter inductor to determine whether the inductor parasitics played a role in the discrepancy. The DPT overshoot measurements were comparable to the results with the first inductor, meaning the inductor parasitics have little impact in the power loop parasitics. Further observation between differences in the two setups revealed that the V_{ds} measurements were slightly different. Measurements in both converter and DPT were taken using Textronix TPP0850 high voltage probes with 800 MHz bandwidth. In the DPT, BNC connector and tip-adapter was used, placed very near to the device and using short, kelvin source traces to the BNC

Table 3.2. Comparison between DPT and converter setup.

DPT	Converter	Potential Impact
Hot plate with insulated surface and thermal blocks	Heatsink, sometimes grounded, with insulating thermal pads	Capacitance to ground
Grounded at low-side Source terminal	Grounded at dc midpoint	Capacitance to ground
Load inductor	Line/EMI filter	Load current stability during transient, EPC of load
Passive probes on gate and drain with tip adapters	Passive probe on drain with leads on tip adapter	High-speed measurement accuracy/resonance
Current shunt (also tested with no shunt)	No current shunt	Loop inductance
DC bus capacitors designed for DPT	DC bus capacitors designed for converter	None expected (similar ratings and values, both electrolytic)
5 ceramic decoupling capacitors, vertically mounted		No difference

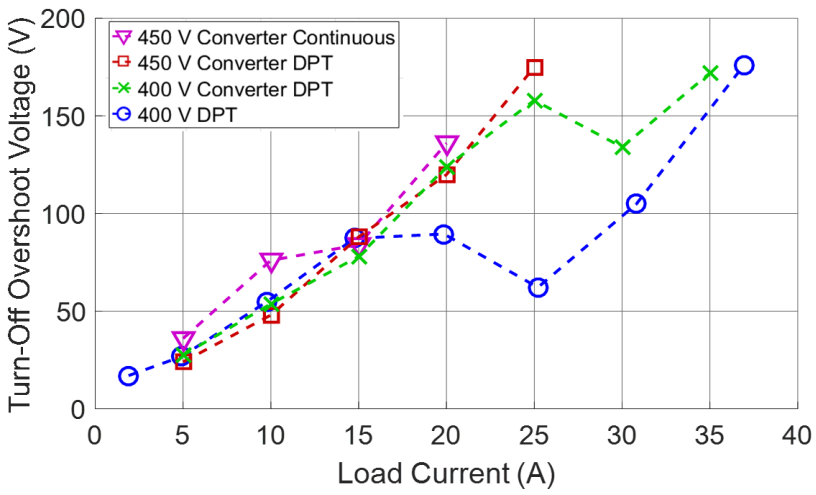


Figure 3.24. Comparison of overshoot voltage between converter continuous and DPT operation and original DPT results.

connector. In the converter, the interface board is positioned directly above the devices in the converter, and the BNC connector required twisted wires be soldered to the leads of the connector before being soldered to the drain and source of devices. The difference between both setups can be seen in Figure 3.25. In order to determine whether the additional wires were affecting the converter measurements, twisted wire pairs were also soldered onto a BNC connector and soldered to the devices on the original DPT board. The DPT was performed, and the results are shown in Figure 3.26. It is clear that both adding and lengthening the wires affects the measured overshoot voltage, even with twisted pairs. In fact, the measurement taken with the 2" additional wires are very similar to our converter overshoot measurements.

In conclusion, not only does size of the measurement loop affect the overshoot measurement but also the length of the wires added to the probe connector, which is a common practice in converter testing. Even with the wires soldered in twisted pairs, the error in measurement is clear.

3.5 Summary

A complete static and dynamic characterization was conducted on the 600 V/30 A GaN GIT devices. From the static characterization, the gate drive current needed to reach the gate forward voltage, V_f, was determined to be at least 5 mA. However, operating above the forward voltage knee of ~3 V with I_g > 10 mA proved to reduce the R_{dson} by 5%. Therefore, the gate current for this design was chosen to be 20 mA, as the decrease in R_{dson} beyond this current is negligible and will further increase gate drive loss. Dynamic

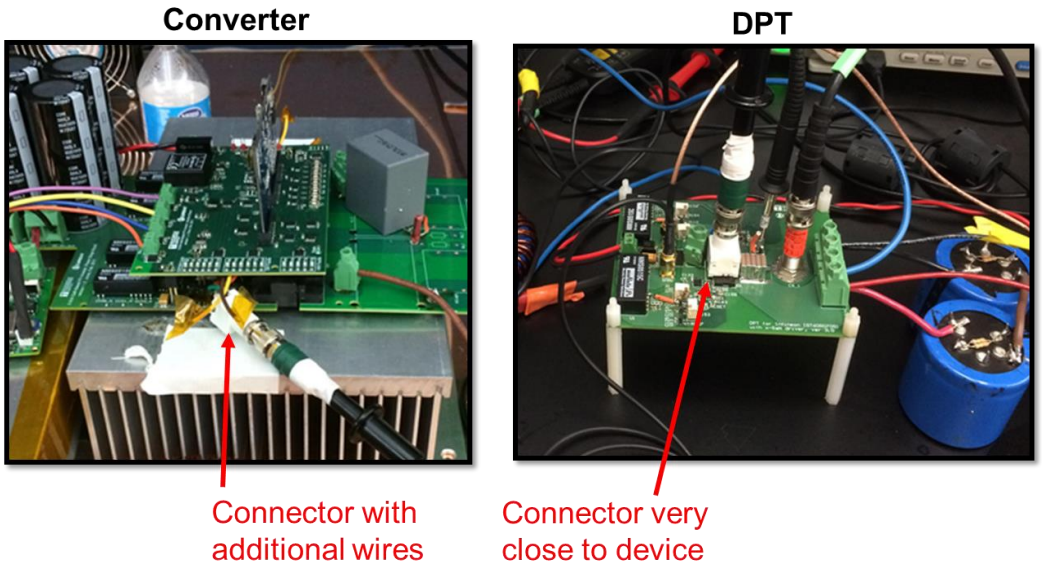


Figure 3.25. Comparison of V_{ds} measurement strategies between converter and DPT setups.

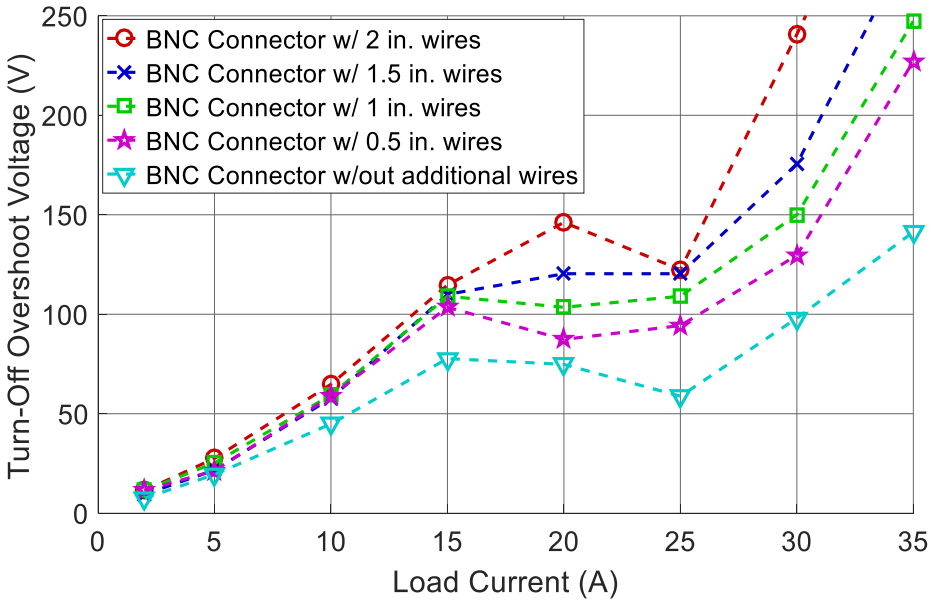


Figure 3.26. Comparison of overshoot measurements taken with various lengths of additional wires soldered to BNC connector.

characterization results were used to observe the impact of gate drive parameters, package parasitics, and PCB parasitics on device switching loss and overshoot voltage. Testing revealed that increasing the turn-off resistance has no positive impact on switching behavior. Therefore, 0 Ω was deemed the optimal turn-off resistance.

Although the package parasitics of the top-cooled device are larger than the bottom-cooled package of the same device, the power loop inductance was decreased by 50% by utilizing the top-cooled package due to the vertical loop layout. A new sweep of C_{su} and V_{dr} determined that the turn-on *di/dt* could increase from 10 A/ns to 17 A/ns while remaining below the 600 V rating. However, the gate parasitics of the top-cooled device resulted in higher turn-on switching loss despite the increased *di/dt* margin. Although switching loss is higher, the cooling of top-cooled package proves to be more efficient and results in other benefits in converter design. Finally, full-scale converter testing revealed discrepancies in the overshoot voltage measurements compared to DPT results. Investigation of the DPT shows that measurement technique of V_{ds} is very sensitive to length of measurement traces, which should be as short as possible for accurate voltage measurements.

Chapter 4

Dead Time Loss Analysis and Modeling

4.1 Introduction

Research has shown that the reverse conduction loss in lateral GaN transistors is typically higher than that of a MOSFET body diode due to the lateral device's gate-dependent voltage drop during reverse conduction. This places further importance on the dead time setting in converters utilizing lateral GaN devices, such as the GIT, as opposed to arbitrarily setting a safe dead time without analysis of the impact on efficiency. Additionally, the analysis of these losses becomes more complicated in GaN-based voltage source inverters (VSI) as compared to DC-DC converters. Unlike in the DC-DC case, the VSI loss model must take into consideration the average of dead time loss over an AC line cycle, where the dead time loss mechanism differs in the light current region than that at higher current. The weight of both light load and heavy load dead time related loss on converter efficiency depends on the RMS load current, bus voltage, and the dead time duration. Additionally, the dependence of dead time loss on junction temperature is considered as part of the optimization strategy since the increase in channel resistance can affect the dead time loss at high load current.

4.2 Dead time loss mechanisms

The dead time is defined as either *turn-on* or *turn-off* depending on the state of the active device, or the hard-switching device, in the phase leg configuration of the VSI. The loss mechanisms of each of these transients are different for the two defined intervals, and therefore, the loss models, $E_{dt,on}$ and $E_{dt,off}$, are developed separately. In Figure 4.1 is an

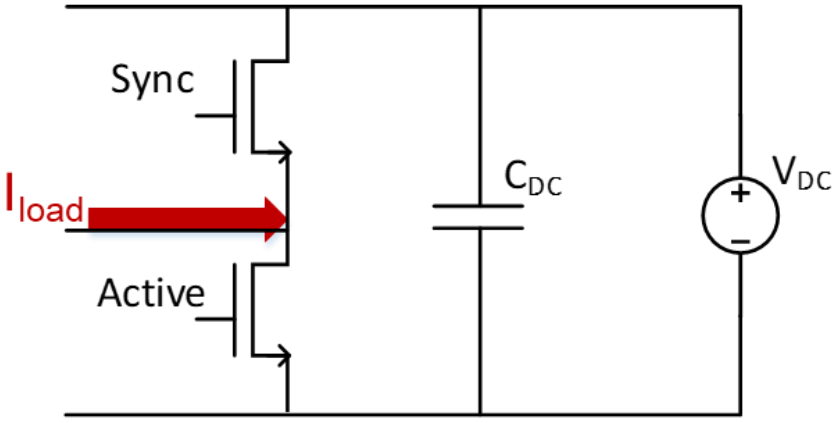
example of these two intervals, with the top waveform being the gate voltage of the high-side synchronous device, and the bottom being that of the low-side active device.

The beginning of the turn-off transient occurs the moment the gate-voltage of the active device falls below the threshold voltage. At this time, the channel of the device turns off, and the load current begins commutating to the synchronous device. This involves the displacement of the charges stored in the equivalent parasitic output capacitance of the two transistors, or $C_{oss,eq}$. After these charges are displaced, the load current will conduct through the channel of the synchronous switch in a similar way to that of a free-wheeling body diode of a MOSFET. During the remainder of the dead time, the synchronous device is still in the off-state and will exhibit higher reverse conduction loss than when the channel is enhanced.

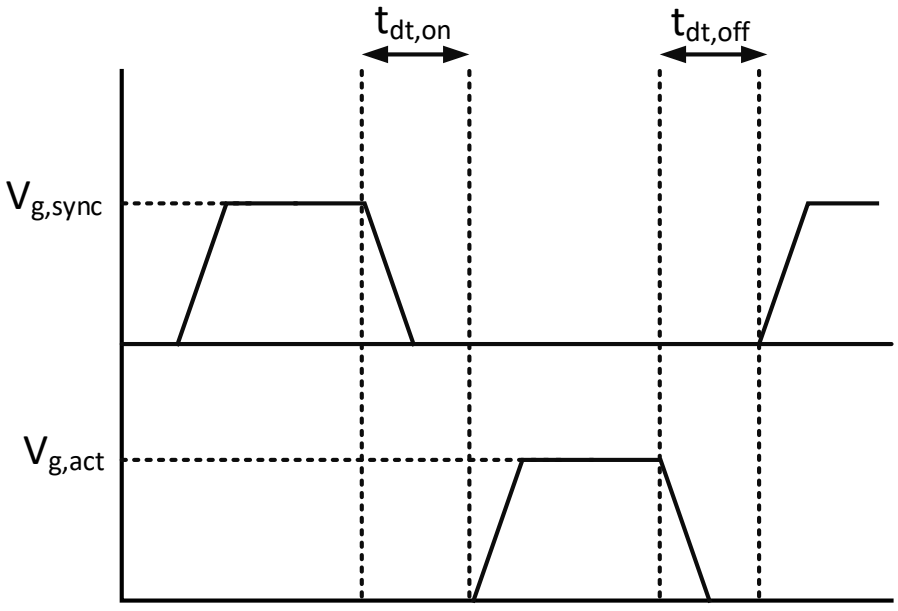
In order for this to occur, C_{oss} must be fully discharged before the end of the dead time. The approximate time in which it takes to discharge the output capacitance is shown in (4.1). Because discharge time has an inverse relationship with the load current, the higher I_L, the more likely commutation will complete before the end of the dead time. An example of this transient is shown in Figure 4.2, with t_{comm} being the commutation time, t_{cond} the reverse conduction interval, and t_{dt} the total dead time.

$$t_{comm} = \frac{C_{oss}(v)+C_p}{I_L} V_{bus} \quad . \tag{4.1}$$

The other scenario possible during *turn-off* occurs when the load current is not high enough to fully discharge C_{oss} before the end of the dead time. If this is the case, then the synchronous switch will turn on with a positive voltage across the drain and source,



(a)



(b)

Figure 4.1. (a) Phase leg of VSI with load current going into the switch-node, and (b) timing sequence of active and synchronous gate driver voltages.

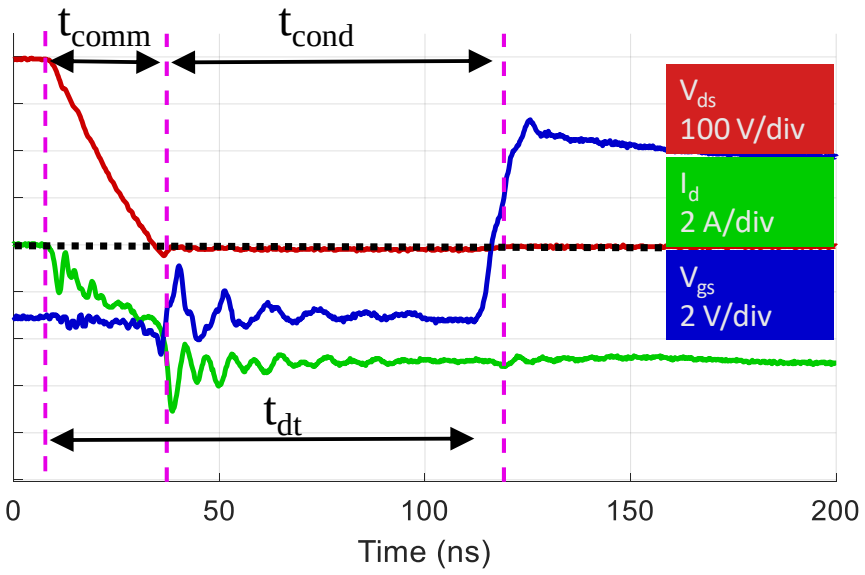


Figure 4.2. Reverse conduction waveforms after turn-off of active device under heavy load with V_{DC} = 400 V, I_L = 35 A, and t_{dt} = 100 ns.

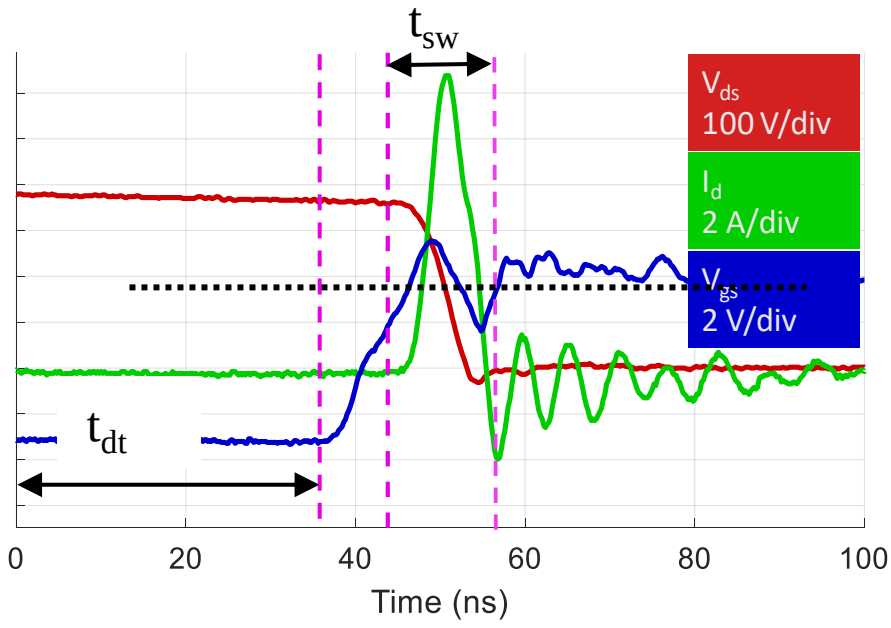


Figure 4.3. Partial switching waveforms during turn-off of active switch and turn-on of synchronous switch under light load with V_{DC}= 400 V, I_L = 0.5 A and t_{dt} = 100 ns.

resulting in a hard-switching transient and additional switching loss. An example of this scenario is shown in Figure 4.3, with t_{sw} being the interval of switching loss and $t_{dt} < t_{comm}$. In DC-DC operation, this loss is seen for low operating currents and can be avoided at higher load currents. In the inverter, these losses are unavoidable for all operating conditions because of the alternating load current about the zero axis. For higher RMS load currents, both loss mechanisms are observed in one line cycle. For very light RMS currents, it is possible for all switching cycles to result in partial ZVS.

The beginning of the *turn-on* transient occurs when the gate voltage of the synchronous device falls below the threshold voltage, and the channel of the synchronous device turns off. During the remainder of the dead time after this transient, the device channel continues to conduct the load current in third quadrant operation. Because no current commutation occurs at this time, the dead time loss is purely reverse conduction loss. Therefore, the minimal safe dead time required to prevent shoot-through is optimal for this side of the dead-band.

4.3 Dead time loss characterization

Analysis of the dead time loss involves both static and dynamic characterization of the GaN devices. Static testing is performed for the analysis of the I-V characteristics in third quadrant operation while dynamic characterization provides data on the switching behavior of the device (switching loss, current rise/fall time, etc.), which also depends on the gate drive design. To model reverse conduction loss, the gate-to-drain threshold and the reverse on-resistance must be determined from the static characterization results. While the forward I-V curve can be used to extract $R_{ds,on}$, characterization of third quadrant

operation reveals that on-resistance during reverse conduction is not equal to forward on-resistance because of the asymmetrical structure of the device. The reverse conduction characteristic depends on the gate-to-drain threshold as previously discussed, while forward characteristic depends on gate-to-source positive threshold. Because the gate-to-drain distance is higher than gate-to-source, the resistance of the channel during forward and reverse conduction differs slightly. $V_{gd,th}$ was approximated after extracting R_{rev} from Figure 4.4 by manually adjusting the variable, $V_{gd,th}$, in (4.2) until the model matched the measured reverse characteristic. Finally, the junction temperature-dependent reverse characteristics were modeled in Figure 4.5 and Figure 4.6.

$$V_{sd} = V_{gd,th} - V_{gs} + I_d R_{rev} \quad . \tag{4.2}$$

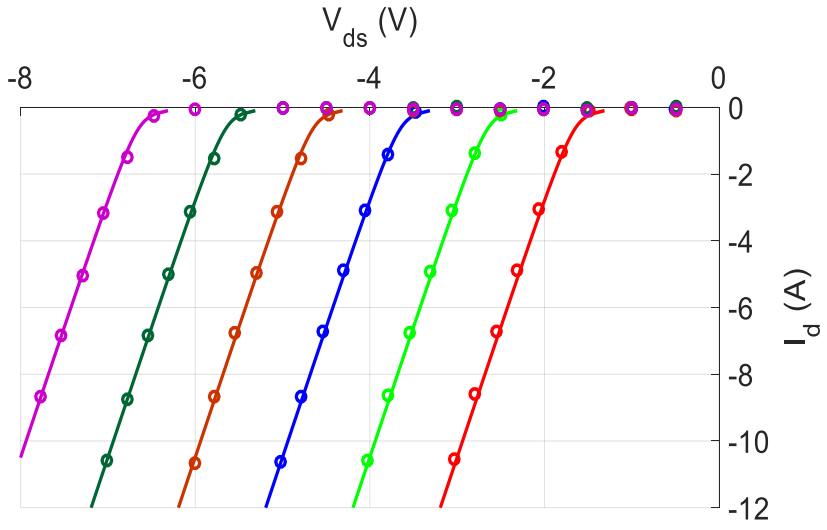


Figure 4.4. Reverse conduction I-V characteristic for various negative gate voltages.

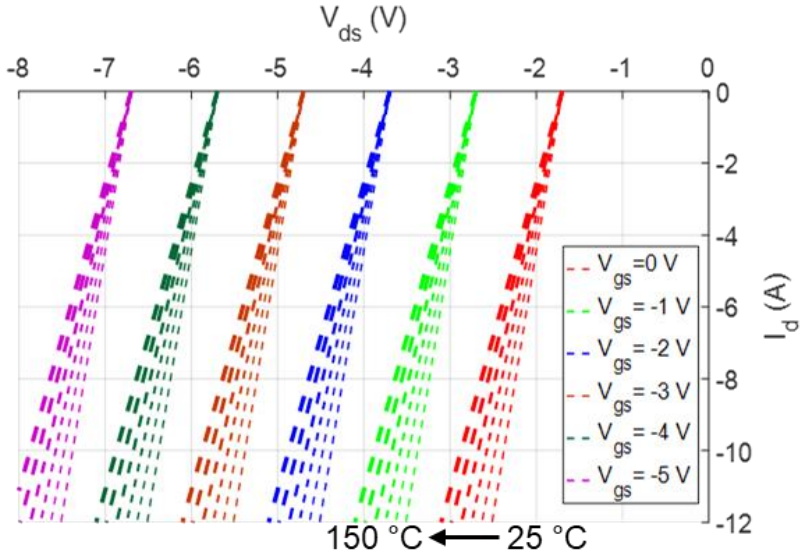


Figure 4.5. Model of junction temperature-dependent reverse conduction characteristic for various negative gate voltages.

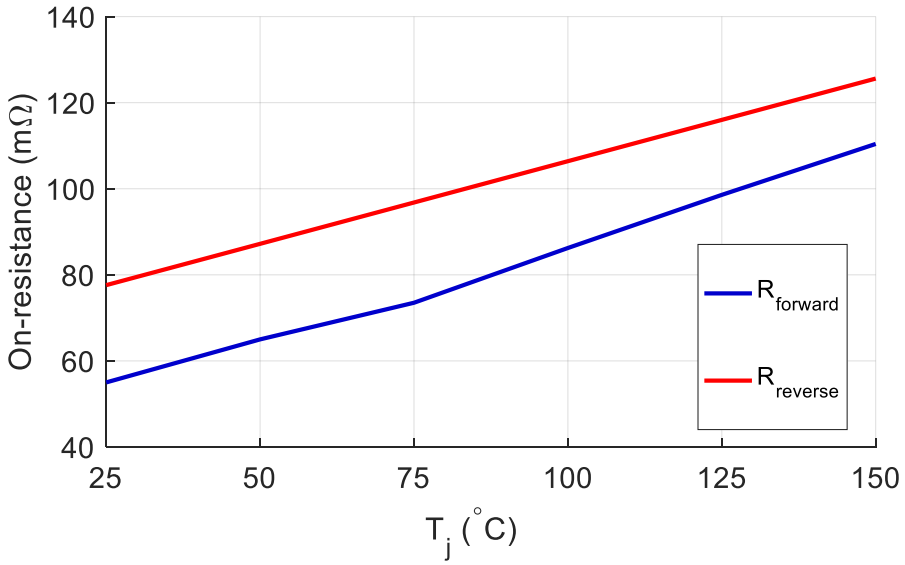


Figure 4.6. Reverse and forward channel resistance vs. junction temperature.

The switching loss in the synchronous device of the phase leg occurs due to insufficient dead time after the turn-off of the active device. Typically in light load conditions, the dead time is insufficient for the load current to discharge C_{oss} before the synchronous device is turned on. To characterize these losses, the gate drive and DPT was designed and configured to that of [49]. The synchronous device was initially left in the off-state for the entire switching transient in order to characterize the current commutation time after active device turn-off as a function of load current. This t_{comm}, shown in Figure 4.3, was developed by measuring the drain current and voltage of the active device over various operating conditions (load current, bus voltage, and junction temperature) and includes both turn-off delay time and voltage fall time. To measure the switching loss due to insufficient dead time, the drain voltage and current of the synchronous device was measured under light load conditions for various dead times.

The dead time was varied from 100 ns down to 5 ns and is shown in Figure 4.7. Based on datasheet values and experimental verifications of turn-off/turn-on time and delay time, a minimum dead time of 5 ns was determined to be sufficient to prevent shoot through for this device up to 35 A. These values are also dependent on the gate drive design (switching speed, propagation delay, etc.), load current, and junction temperature [48, 79], and some safety margin should be taken into consideration. For the gate drivers used in this experiment, a propagation delay of 50 ± 15 ns was observed. Although the impact of junction temperature on dead time loss has not been considered in the literature, it will impact the reverse conduction loss as channel resistance increases due to junction

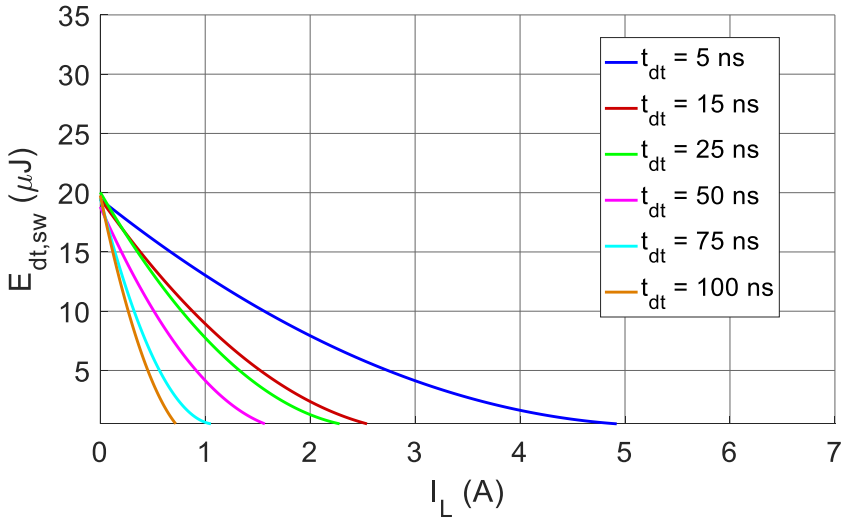


Figure 4.7. Switching loss incurred in synchronous device due to insufficient dead time with V_{DC} = 400 V.

temperature. To characterize the impact of junction temperature, the devices were tested from 25 °C to 150 °C in 25 degree intervals for both static and dynamic characterization.

The results in Figure 4.6 and Figure 4.8 show the impact of junction temperature on reverse conduction loss and channel resistance respectively. Additionally, Figure 4.6 reveals a higher reverse on-resistance than forward, meaning conduction loss will be higher during reverse conduction, especially for negative gate voltage. Figure 4.8 shows the impact of junction temperature on both partial switching loss and reverse conduction loss collectively. This figure also shows that the impact of junction temperature on the dead time related switching loss is not as significant as the reverse conduction loss. One reason is that the current is already less than 5 A, where the switching loss is already low, and C_{oss} is partially discharged, meaning V_{ds} is lower. Additionally, impact of junction temperature on commutation time is not significant as the gate drive turns the device off very quickly.

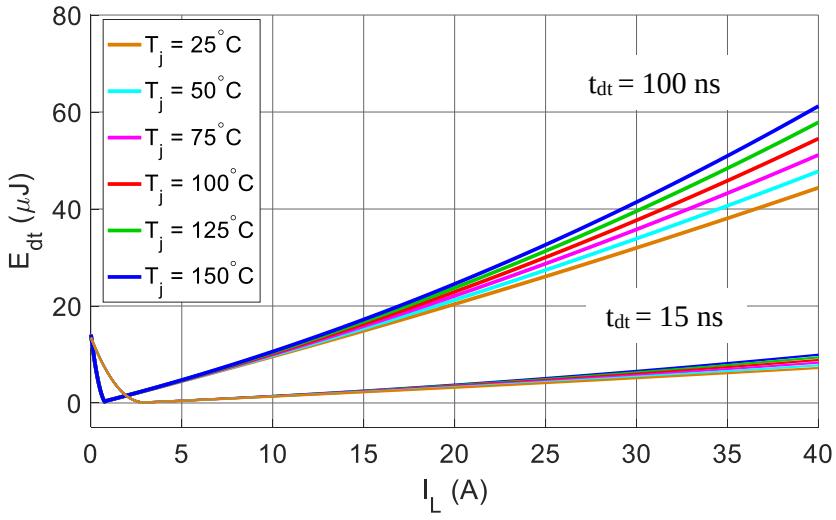


Figure 4.8. Impact of junction temperature on dead time loss vs. load current and dead time.

The main contributor to commutation time is load current and device parasitic capacitance, which is not temperature dependent.

4.4 Dead time loss modeling

Using a combination of this data with a model of turn-off time obtained from the DPT of active device turn-off, a complete model is made from the switching loss calculations and the reverse conduction calculations. The final equations are shown in equations (4.3)-(4.6). The instantaneous dead time loss versus load current is in Figure 4.9, and the average loss over various AC line cycles is in Figure 4.10. If the ripple current, ΔI_L, is non-negligible compared to the load current, I_L, then the instantaneous current at the maximum and minimum of the ripple current, $I = I \pm \Delta I_L$, for each switching cycle should be averaged along the line cycle, not I_L. For this application, with a maximum ripple current of ~10 A, taking the ripple current into consideration shows a difference of < 1 W compared to assuming no ripple current (Figure 4.11). Because dead time loss occurs every switching

cycle, the power loss in Figure 4.12 is displayed as a ratio of the total hard-switching loss of the active device. The results show that for 100 ns dead time, the loss already contributes between 20 to 50 percent depending on the bus voltage. This can be reduced to less than 10 percent if the dead time is reduced. However, for lower dead time and light load, the loss is dominated by partial switching loss, and greater than 20 percent additional switching loss is induced.

$$\mathrm{E_{dt,sw}} = \mathrm{f(V_{bus}, T_j)I_L}^2 + \mathrm{g(V_{bus}, T_j)I_L} + \mathrm{h(V_{bus}, T_j)} \ . \tag{4.3}$$

$$E_{dt,off} = (t_{dt} + t_{on,delay} - t_{off,model})((V_{gd,th} - V_{gs}) \cdot I_L + {I_L}^2 \cdot (R_{rev}(T_j) - R_{on}(T_j))) \tag{4.4}$$

$$E_{dt,on} = (t_{dt} + t_{on,delay} - t_{off,delay})((V_{gd,th} - V_{gs}) \cdot I_L + {I_L}^2 \cdot (R_{rev}(T_j) - R_{on}(T_j))) \tag{4.5}$$

$$E_{dt,ave} = \frac{1}{\pi}\int_0^{\pi} E_{dt,total}(V_{dc}, T_j, \sqrt{2}I_{grid}sin(\varphi))d\varphi \tag{4.6}$$

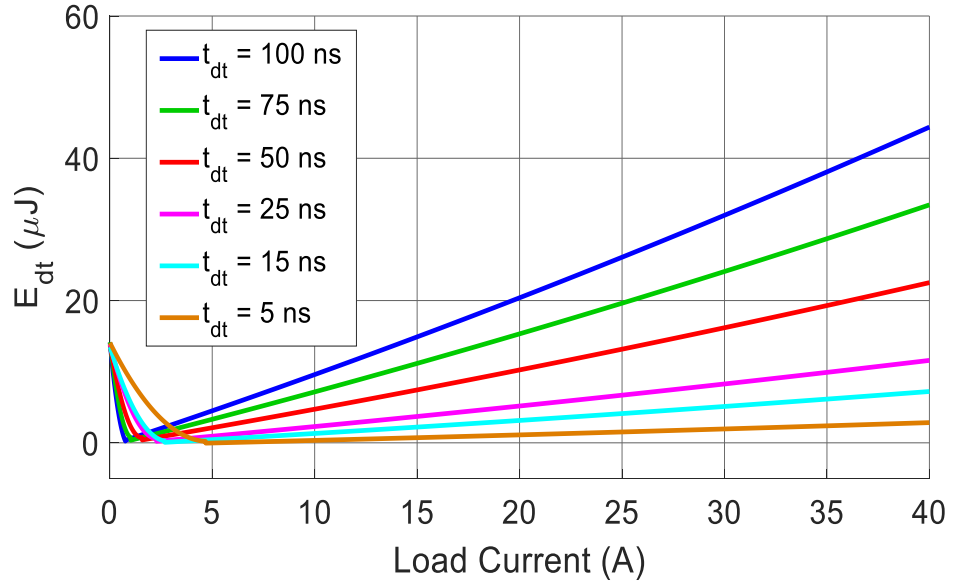


Figure 4.9. . Instantaneous dead time loss vs. load current and dead time of GaN GIT with V_{DC} = 400 V.

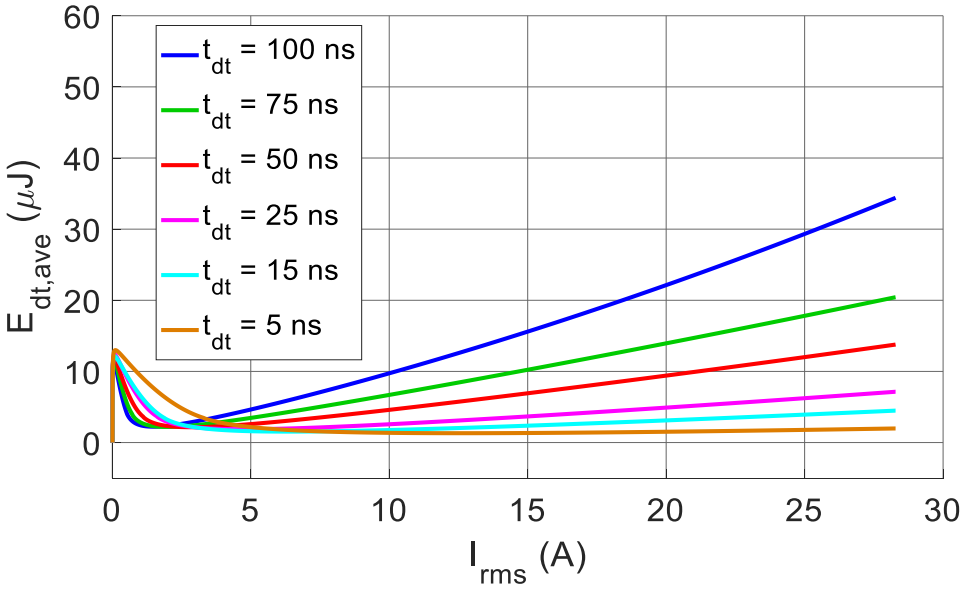


Figure 4.10. Average energy loss due to dead time over AC line cycle vs. RMS current and dead time with V_{DC} = 400 V.

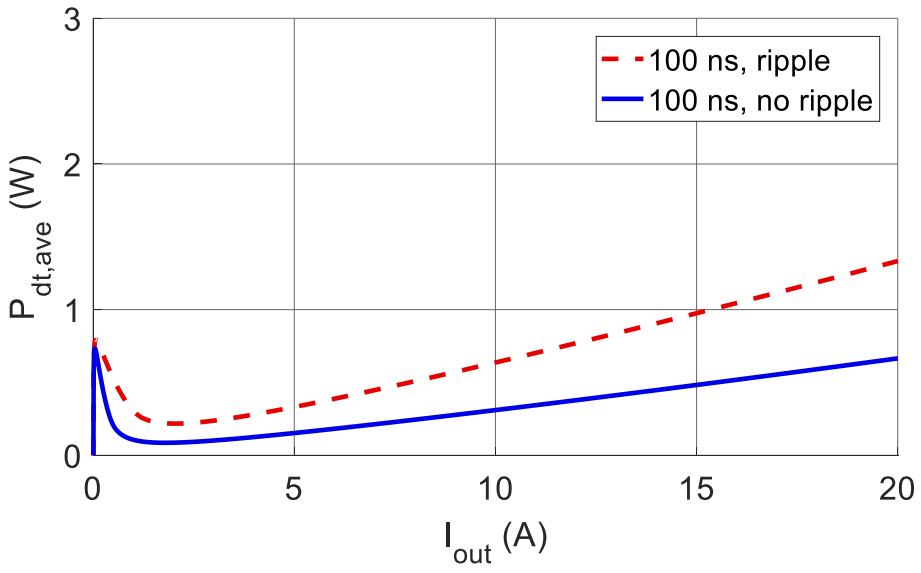


Figure 4.11. Impact of ripple current consideration of dead time loss analysis for V_{bus} = 400 V and dead time = 100 ns.

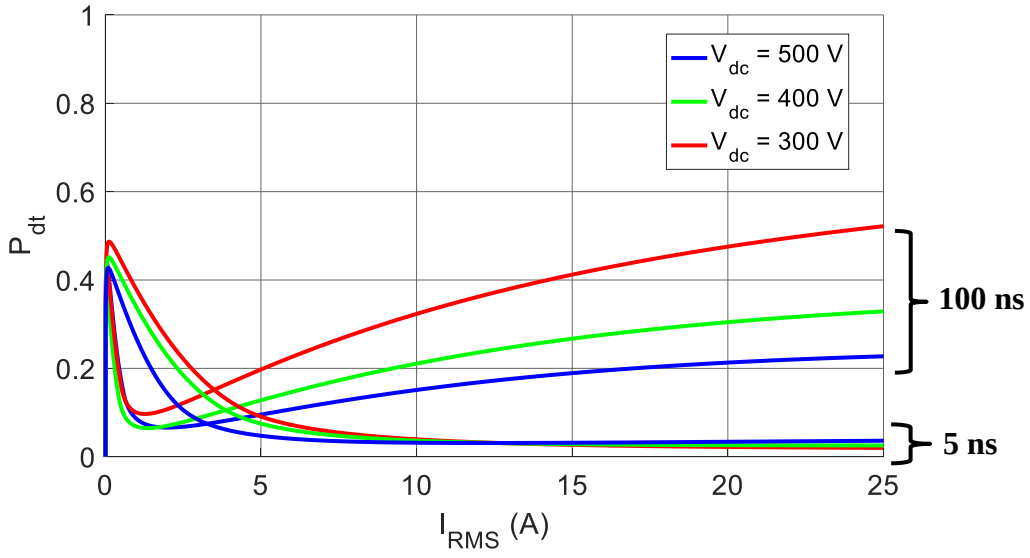


Figure 4.12. Additional average switching loss due to fixed dead time vs. bus voltage and dead time.

4.5 Dead time loss optimization

Unlike the DC-DC case, with a fixed dead time in the inverter, dead time loss is unavoidable because of the zero current crossing. However, for each line cycle current, there does exist a dead time that will result in the lowest loss. The plot in Figure 4.12 shows that above a particular line cycle, the optimal dead time begins to decrease to the minimal dead time, whereas below this point, the optimal dead time begins to increase due to the increased weight of switching loss in the average loss.

The dead time that results in the lowest loss per RMS current is shown in Figure 4.13, and the corresponding optimal dead time for instantaneous current is compared (instantaneous). The adaptive scheme is based on Figure 4.9 and can be used to adapt the dead time each switching cycle as a function of measured load current. In Figure 4.13**,** the optimal dead time in the adaptive scheme is always lower than the AC-DC case because both partial switching loss and reverse conduction loss do not have to be considered. It was also observed that the slower the commutation time and the more partial switching loss in a line cycle, the higher the optimal dead time for each RMS current.

To reduce dead time loss in the inverter, two options are available: dead time loss elimination using adaptive dead time scheme strategies or fixed dead time based on loss trade-off over various dead times and operating conditions. The benefit of adaptive dead time is virtual elimination of dead time loss but at the expense of control computation time and/or additional circuitry [80], [81-83]. Figure 4.14 shows the benefit of incorporating adaptive dead time, with a cutoff of 200 ns. This means if the commutation time is greater than 200 ns, partial switching loss will be unavoidable. However, for instantaneous current

greater than ~0.5 A, the dead time loss can be eliminated. Figure 4.15 shows that at light load, adaptive dead time can save more than 10% total loss, since the dead time related loss makes up a larger portion of total loss at this power level. Whereas at higher load, conduction loss is the main contributor, and dead time loss is a small portion in comparison, and 1% loss can be saved using adaptive dead time.

4.6 Experimental verification

First, a fixed dead time scheme was implemented in a 5 kW, GaN-based, full-bridge inverter with a switching frequency of 140 kHz. As switching frequency is increased, these losses are expected to scale linearly, and the contribution to total converter loss will increase. It is also important to note that the effective dead time will not be equal to the dead time programmed in the control because of the propagation delay of the controller

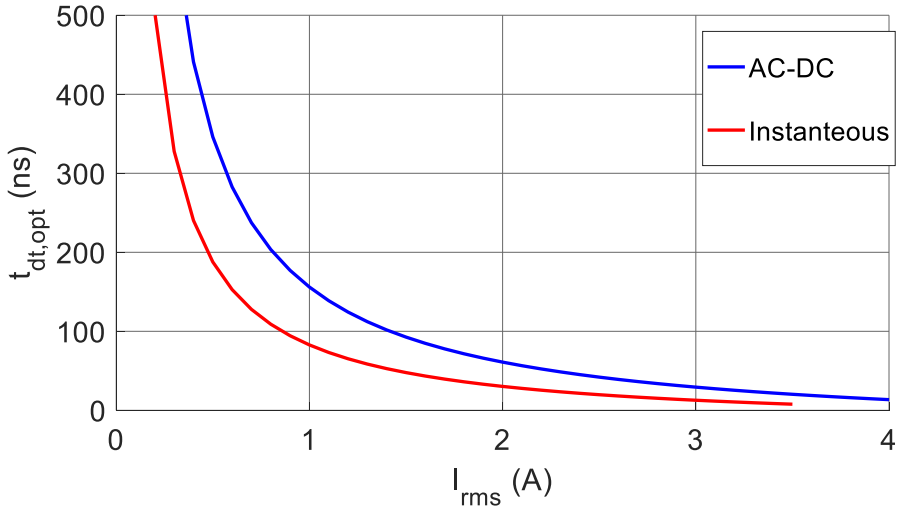


Figure 4.13. Optimal dead time for AC-DC RMS load vs. optimal dead time for instantaneous load current.

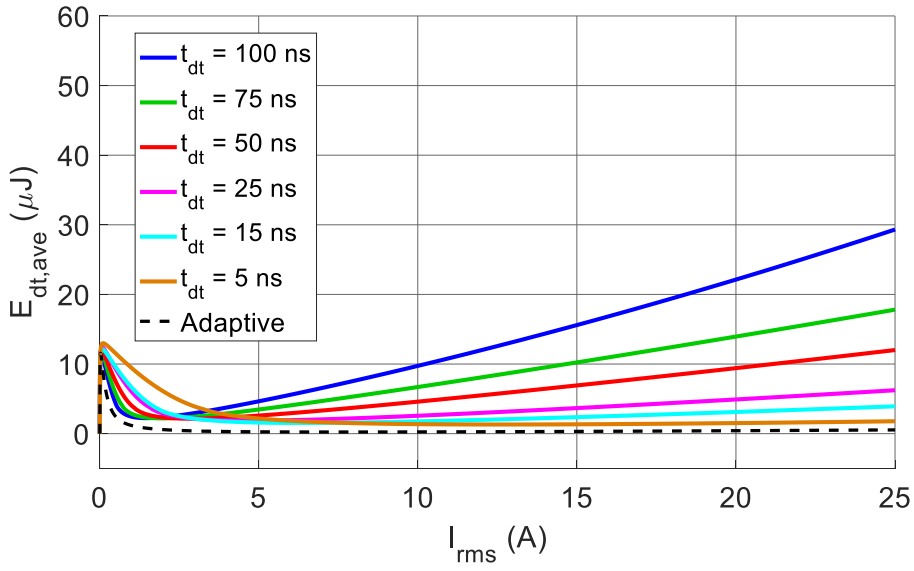


Figure 4.14. Benefit of adaptive dead time vs. fixed dead time setting and RMS load current.

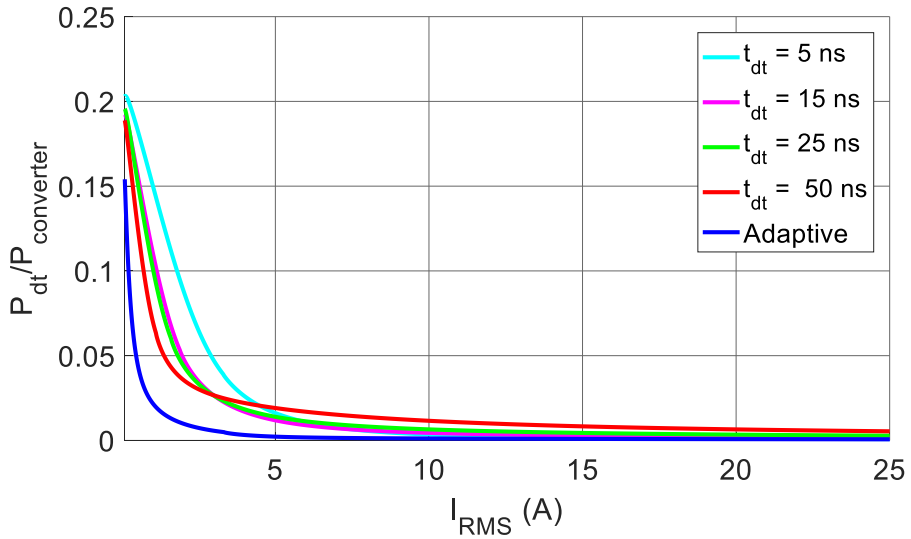


Figure 4.15. Contribution of dead time loss in total inverter loss with fixed dead time compared to adaptive dead time with a 200 ns cutoff at light load and 5 ns cutoff for high load.

and gate driver. The designer should also consider the mismatch in propagation delay between the high-side and low-side devices [79]. For this reason, some safety margin should be considered, especially if the dead time is small. In this experiment, the effective dead time was verified by measuring the gate-to-source terminals of the low-side and high-side devices. Figure 4.16 shows the full setup of the experiment, and Figure 4.17 shows examples of the input and output waveforms. Tests were first conducted at 500 W, 1000 W, and 2500 W, and the dead time was varied from 200 ns down to 5 ns to verify the dead time curve in Figure 4.13 for AC-DC case. The power loss was calculated from measurements shown on the power analyzer, and the results of the test are shown in Figure 4.18. The dead time resulting in the lowest loss for each of these power outputs were compared to the results in Figure 4.13 and plotted in Figure 4.20**.**

The results match very closely for 100 ns and 5 ns. However, the measured optimal dead time was higher in the medium-current range, with 25 ns being the optimal measured dead time versus the predicted 15 ns. One possibility is that at 4 A $I_{rms,}$ the dead time loss is already close between 25 ns dead time and 15 ns dead time, less than 0.5 W difference. The error of power analyzer at this current is ± 2 A. Therefore, the difference in measured power loss is within 2 A. The other possibility for optimal dead time discrepancy is the presence of additional parasitic capacitance not taken into consideration in the model. Although the power stage is very close to that of the DPT setup, there is additional stray capacitance from load inductor and heatsink.

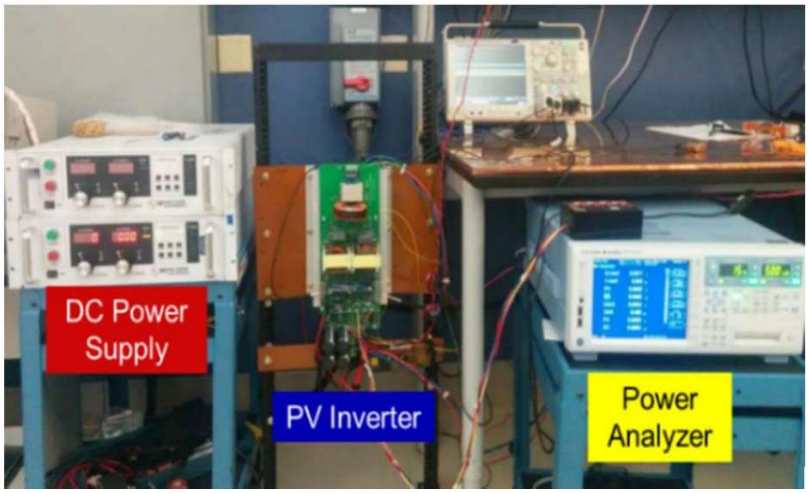


Figure 4.16. Inverter test setup.

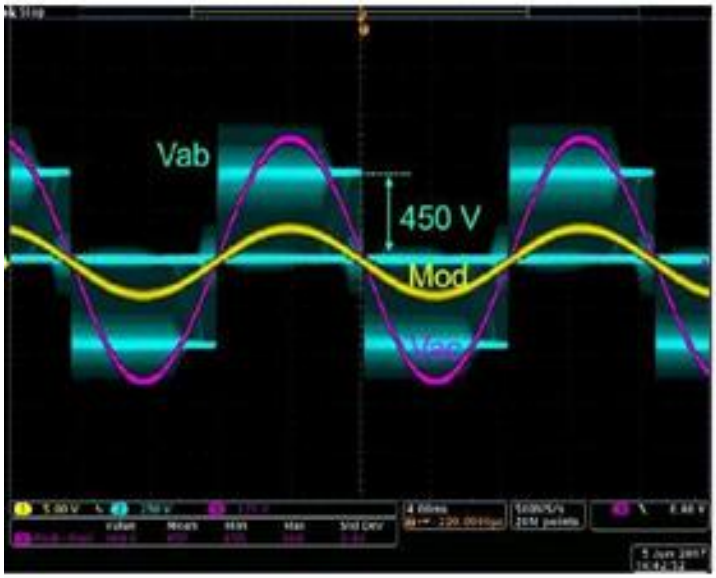


Figure 4.17. AC steady-state waveforms with 450 V in, 230 V out, and 140 kHz f_{sw}

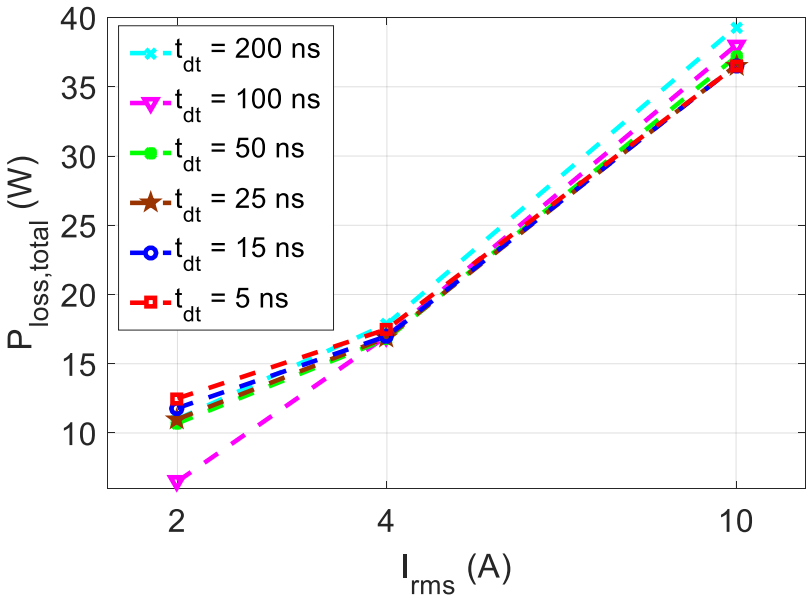


Figure 4.18. Converter loss vs. dead time for GaN-based inverter with V_{dc} = 400 V and V_{out} = 230 V_{rms}.

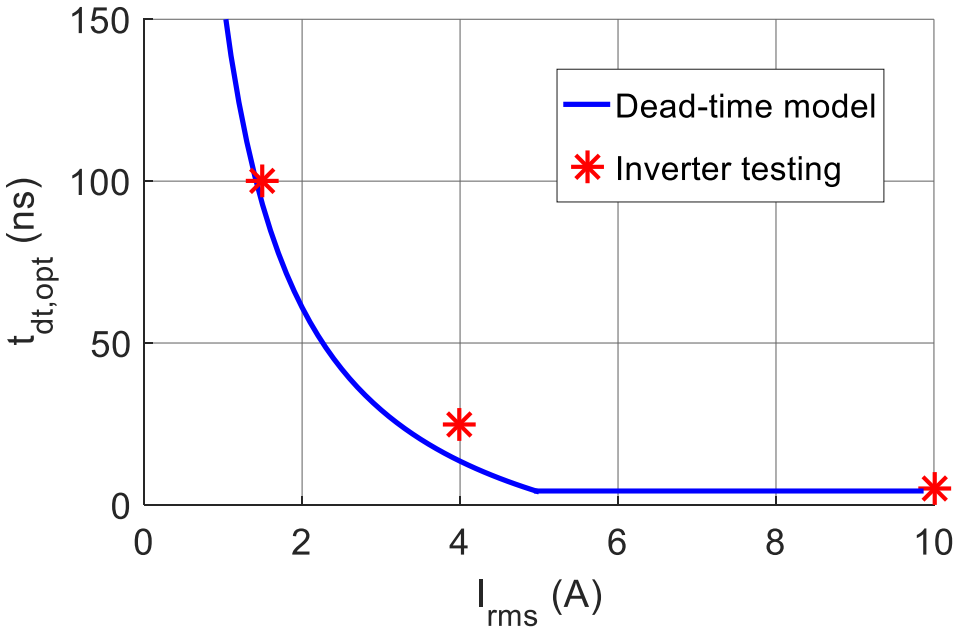


Figure 4.19. Optimal dead time model vs. line cycle current compared to optimal dead time based on lowest loss in full inverter testing with V_{dc} = 400 V and V_{out} = 230 V_{rms}.

An additional stray capacitance of 70 pF was calculated and measured from heatsink connection, load inductor and PCB traces. Figure 4.20 shows the impact of an additional 70 pF stray capacitance to the average power loss with 5 ns dead time. The impact is an increase in both commutation time and partial switching loss due to additional capacitive energy. Equation (4.7) includes the additional stray capacitance in the commutation time calculation. To calculate the results in Figure 4.20, it was assumed that the impact on commutation time did not have a significant impact on the drain voltage at the time of the partial switching event. Therefore, a value of $\frac{1}{2}C \cdot V^2$ was added to the partial switching loss measurement, with C_p being the additional stray capacitance.

$$t_{comm} = \frac{C_{oss} + C_p}{I_L} \cdot V_{bus} \tag{4.7}$$

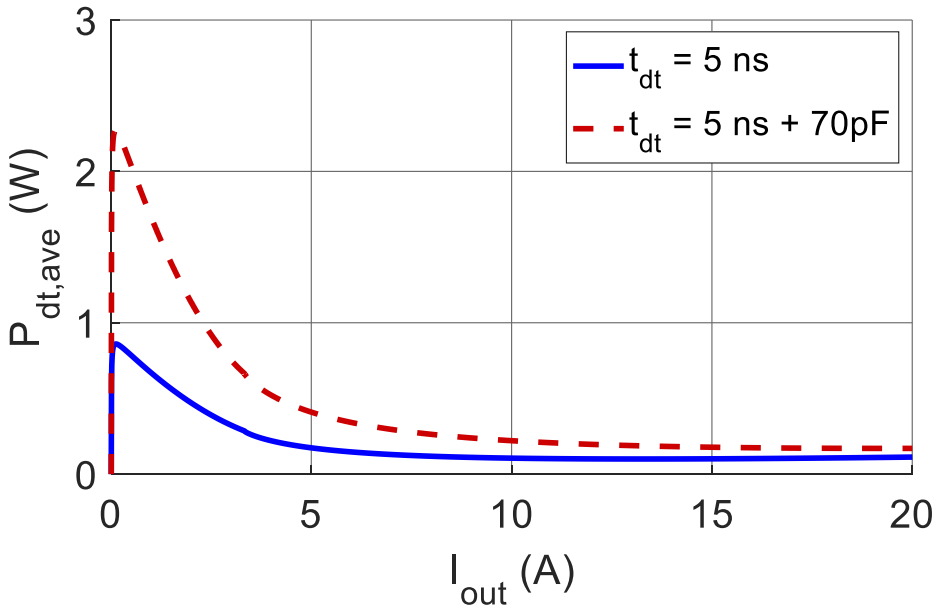


Figure 4.20. Impact of converter parasitic capacitance on partial switching loss with dead time equal to 100 ns and 15 ns.

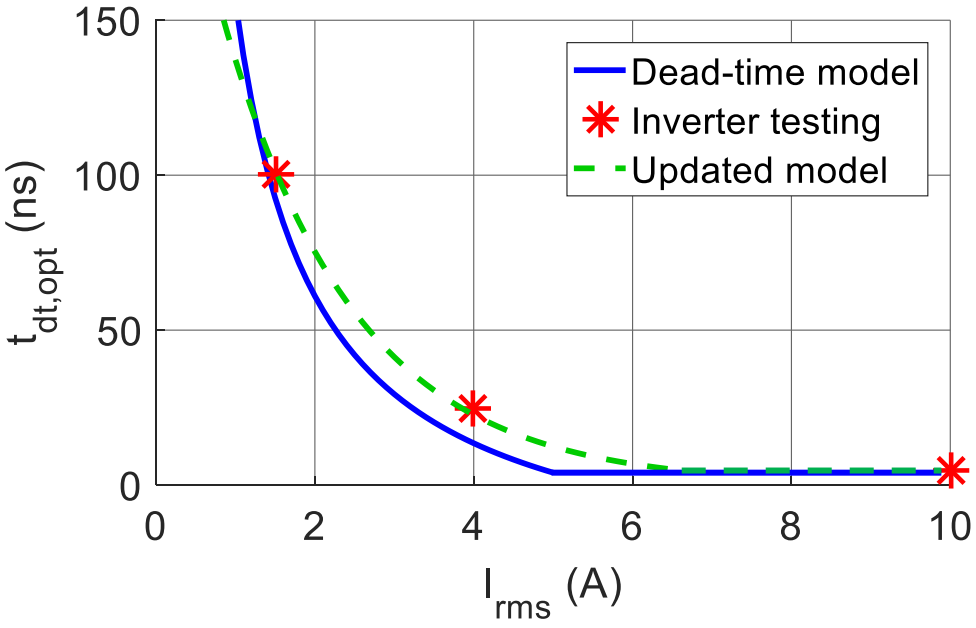


Figure 4.21. Updated optimal dead time model with additional 70 pF stray capacitance.

This additional energy was added to all dead time loss calculations, and an updated optimal dead time curve was developed. From this data, the updated optimal dead time curve was compared to the previous model and to the experimental results. Figure 4.21 verifies how the updated model with the additional stray capacitance matches more closely to the experimental data.

4.7 Summary

The impact of dead time loss in a full-bridge, 4.5 kW inverter was characterized and modeled based on 600 V GaN GITs to determine the significance of various dead times on total converter loss with an AC line cycle. Additionally, a method based on static and dynamic characterization was developed to obtain an optimal fixed dead time based on the trade-off between extra switching loss and reverse conduction loss over the whole

operating range. Depending on the operating range, the results show that dead time can contribute up to 40% additional switching loss with 100 ns dead time for high load current and with 5 ns dead time at low load current. Because the inverter has a changing load, a dead time of 25-50 ns results in a better trade-off between the light load and heavy load loss. The benefit of adaptive dead time was considered, and ~1% of total converter loss would be saved above 5 A I_{rms}. However, more than 10% light load power loss would be saved by implementing adaptive dead time.

Chapter 5

Short Circuit Robustness and Protection Scheme

5.1 Introduction

Recent literature in GaN short-circuit capability has shown that the critical energy of GaN during a short-circuit event is significantly less than that of Si or SiC devices. Compared to Si, the drift region of GaN devices are designed to take advantage of the high electric field breakdown of GaN material, and therefore, a much higher electric field is to be expected when high drain voltage is applied, leading to higher power dissipation density than Si [6]. Likewise, high short-circuit current is more likely to concentrate in the AlGaN/GaN interface rather than the bulk material of a vertical device, causing extreme localized temperature rise. The higher saturation velocity of GaN also results in higher saturation current, further increasing the likelihood of localized temperature surge during a short-circuit event and consequently lower robustness [58]. Particularly, as bus voltage is increased, the critical energy decreases significantly and is not necessarily linear. Studies show that the critical energy drops almost linearly until a sudden sharp decrease occurs above 350 V for a 600 V device [73, 84]. This is important to note when designing short-circuit protection since the worst case operating condition occurs at maximum operating bus voltage.

As discussed in Chapter 2, the most commonly implemented short-circuit protection scheme is desaturation protection, which has been shown to protect the GaN device within 200 ns [76-78]. The main contributor to detection time in these tests was the blanking time, which can be reduced by reducing the blanking capacitor. However,

reducing the blanking capacitor will reduce the noise immunity of the protection circuit, and for high *dv/dt* application like GaN, blanking time becomes more important. Additionally, these studies were conducted on lower than 600 V rated devices and may not be sufficient to protect higher rated devices, in which longer blanking time may be required. An additional downside to desaturation protection is the inability to select a fault threshold current independent of saturation current. This is disadvantageous because for GaN HEMTS, the saturation current decreases with junction temperature, which means the fault current must be higher for room temperature operation to guarantee protection at higher junction temperature. Finally, desaturation implementation requires a sensing diode be placed at the drain of the device, which adds to the total output capacitance.

In [17], a fast overcurrent protection scheme was developed for the GaN GIT, taking advantage of the unique properties of the gate voltage/drain current characteristics of the GIT. The drain current is sensed through an internal resistance from gate-to-source, meaning the gate voltage can indicate what is the drain current, as shown in Figure 5.1. Equation (5.1) explains the dependence of $V_{gs,ext}$ on I_d. Because the gate current is very low, in the milliamps range, it was originally ignored in the estimation in (5.2). However, further studies in this thesis will show that the gate current will have significant impact on the protection design and reference voltage, which will be explained in future sections.

$$V_{gs} = V_{gs,diode} + (I_d + I_g)r_1 \tag{5.1}$$

$$V_{gs,ss} = V_{gs,diode} + I_d r_1 \ . \tag{5.2}$$

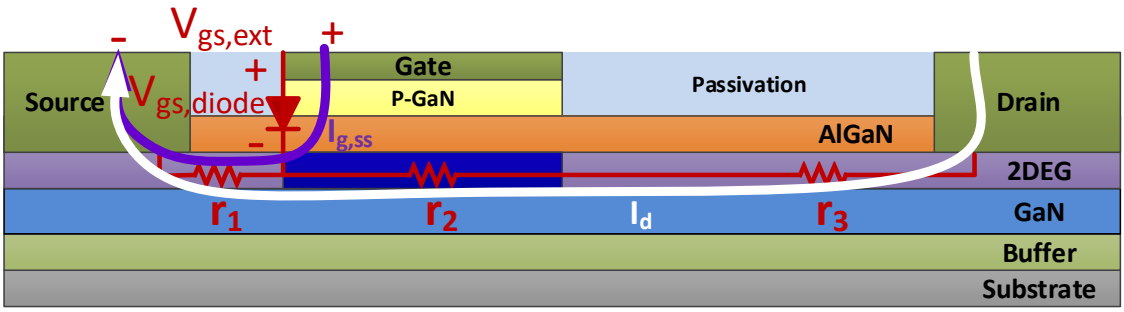


Figure 5.1. Sub-circuit model for GaN GIT, with explanation for I_d-V_{gs} relationship when I_g is fixed [17].

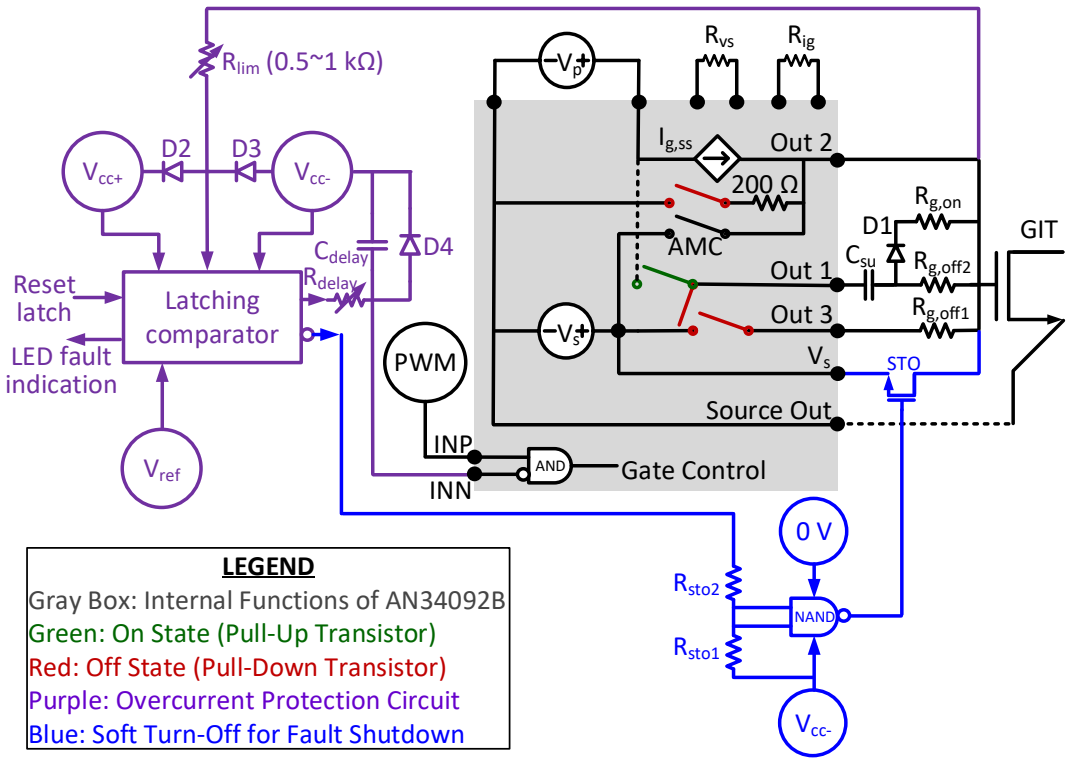


Figure 5.2. Schematic for short-circuit protection utilized in [17].

The advantage of this scheme is the ability to set the fault threshold current independent of junction temperature and in the elimination of the sensing diode required to implement desaturation protection. This protection scheme was also verified to protect the devices in less than 200 ns.

5.2 Short circuit robustness

While the protection scheme was verified to successfully protect the devices up to 125 °C junction temperature without device failure in [17], it is beneficial to know what is the maximum allowable time the device can withstand a short-circuit event. Therefore, both the bottom-cooled and top-cooled 600 V GaN GIT devices underwent destructive testing to observe both critical energy and failure mechanism at 400 V and up to 150 °C. The same DPT setup utilized in Section 3.3 was used to test the devices under short-circuit condition. The load inductor was removed, and the bus voltage was increased from 100-400 V. A HSF was first induced on the low-side switch by turning on the upper device and supplying a short pulse to the lower device. The pulse length was increased until device failure occurred. Table 5.1 shows a comparison of failure time and critical energy between the two device packages. As expected, the critical energy is roughly the same for both devices since the two die are identical, and Figure 5.3 shows a similar failure mechanism for both devices. In Figure 5.3 (a)**,** the time of failure can be seen at time t_1, where the gate voltage suddenly spikes to 8 V. Consequently the drain current also increases to ~160 A, which is 50 A above the normal short-circuit current. This indicates a possible leakage current from drain-to-gate as discussed in the literature. At the same time, the drain voltage

Table 5.1. Short-circuit failure time and critical energy of IGT60R070G1 (bottom-cooled) package and IGOT60R070D1 (top-cooled) package.

	Top-cooled	**Bottom-cooled**	
Bus voltage failure	380V	380 V	400 V
Failure time	315 ns	315 ns	220 ns
Crit. energy	7.7 mJ	7.7 mJ	6 mJ

reduces to approximately 100 V, indicating failure of the device channel to continue blocking the full bus voltage.

After short-circuit failure, all pins failed short for the HSF device. It isn't until ~2.7 μs that the gate-to-source appears to fail. The upper device survives the test since the critical energy is much lower in the FUL case. Based on this information, the protection time should be less than 215 ns to successfully protect the devices before failure. The results from Figure 5.4 also show that the margin to protect devices after 200 ns is very short as the device failure actually happens after turn-off. At time t_1, the device is turned off 210 ns after short-circuit. However, device failure happens at t_2, ~30 ns after turn-off. At this point, the short-circuit energy is already 6 mJ, the critical energy at V_{dc} = 400 V.

According to [85], the critical energy is likely to decrease with elevated junction temperature. However, high-temperature critical energy testing during this study was inconclusive. At 150 °C and 400 V bus voltage, the device survives testing even up to 4.5 μs with no indication of failure. However, after cooling the junction temperature to room

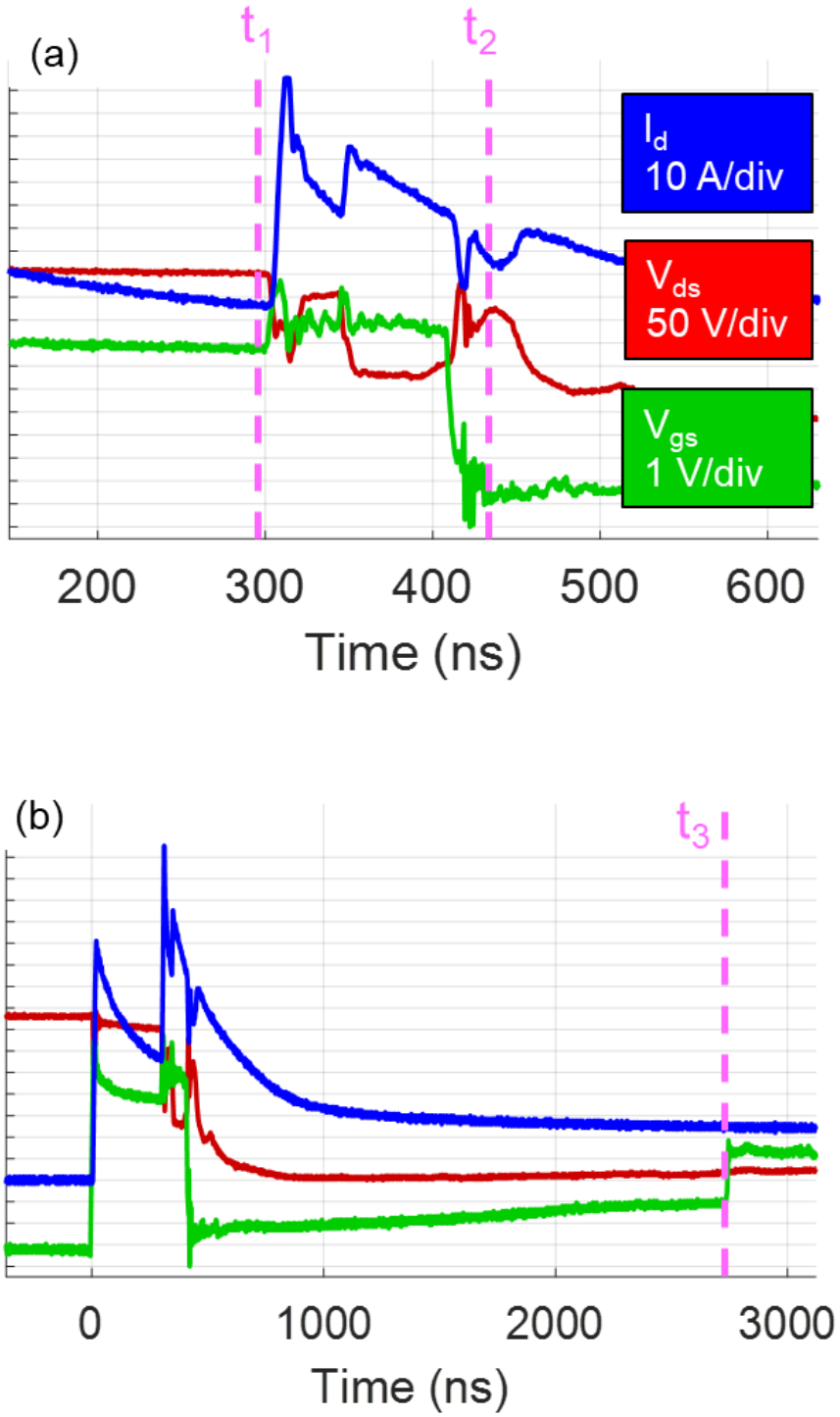


Figure 5.3. Short circuit failure for top-cooled device at V_{dc} = 400 V.

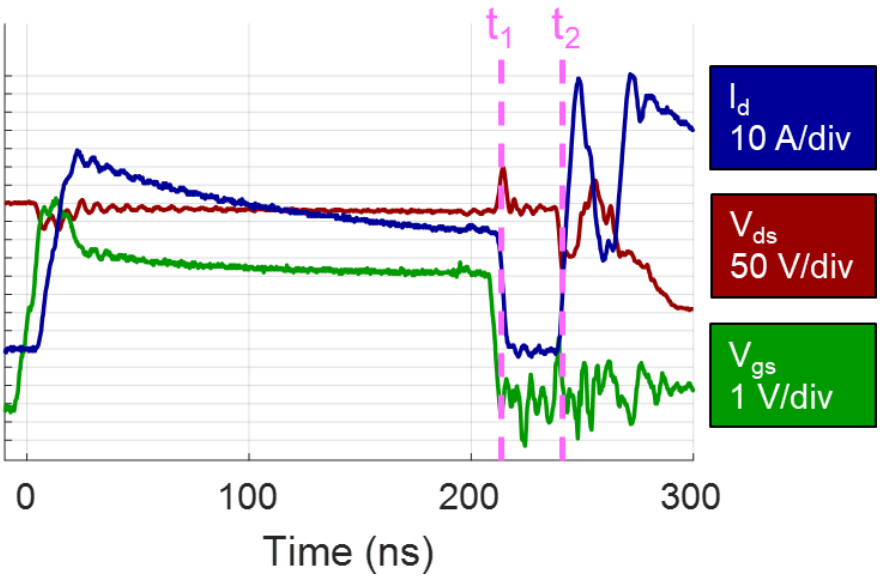


Figure 5.4. Short-circuit failure after turn-off with V_{dc} = 400 V.

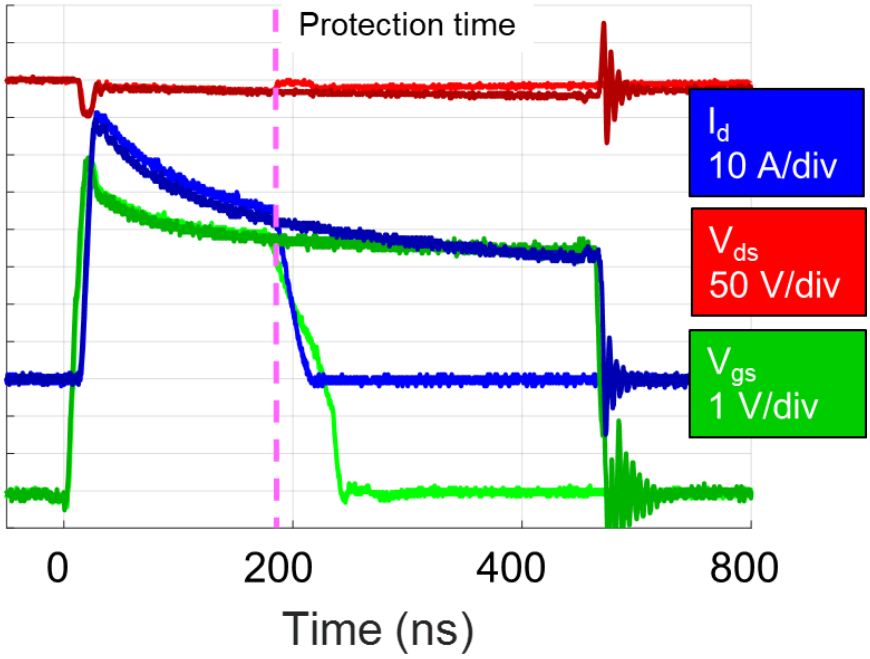


Figure 5.5. Short-circuit capability of device at 150 °C and V_{dc} = 400 V with the light curves representing protection implementation and the dark curves representing a 400 ns pulse without device failure.

temperature, the device failure occurs after 220 ns at 400 V as prior testing indicates. This behavior may be due to a decrease in maximum short-circuit current, or the increased junction temperature allows a more uniform temperature rise during the short-cricuit. It was shown in the literature that localized elevated temperature may be the root cause of failure in this device. With a higher initial junction temperature, it is possible that the temperature distribution is more uniform. Figure 5.5 shows that the short-circuit current at higher temperature is much lower and closer to the safe operating area of the 30 A device, another possible explanation for the robustness at elevated temperature. A DPT was then conducted after the short-circuit testing at high-temperature, which verified that the devices were not damaged during the 4.5 μs pulse.

5.3 Consideration of device packaging

Implementation of the gate sensing protection scheme for GIT was first implemented on the bottom-cooled package device. The results in [17] verify that the protection scheme successfully protects the device under operating conditions up to 400 V and 125 °C. The protection was then implemented utilizing the top-cooled package to verify the function of the protection under higher *di/dt* conditions and up to 150 °C, which is the device maximum junction temperature rating. This section explores the impact of a faster gate drive speed and lower power loop inductance due to utilizing the top-side cooled package on protection scheme performance.

Because the detection time and short-circuit energy is a function of the *di/dt* and L_{loop}, the short-circuit energy loss is likely to be higher for a shorter amount of time when implementing the vertical power loop with the top-cooled device. In Chapter 3, it was

discussed that the gate drive speed utilizing the top-cooled package can be increased due to the lower power loop inductance and lower overshoot voltage. Therefore, the maximum drain current in the HSF fault case will be higher due to the faster gate drive speed. Additionally, the maximum current will also be higher in the FUL case due to half the power loop inductance, meaning the *di/dt* will be roughly twice as fast as the bottom-cooled design. Fortunately, an advantage of this scheme is that the protection time increases as the *di/dt*. Therefore, improvement of the protection scheme is possible by utilizing the optimized vertical power loop design discussed in Chapter 3.

From the results in Figure 5.6 and Figure 5.7, it can be seen that the HSF and FUL detection times are longer in the bottom-cooled design than in the top-cooled design due to the slower gate drive speed and higher power loop inductance. For the HSF case, the detection time is reduced by ~20 ns by implementing the vertical power loop, whereas the reduction in detection time is much more significant in the FUL case. The detection time for FUL is reduced by ~50 ns by implementing the vertical power loop, and the impact of junction temperature on detection time in the FUL case is less significant in the vertical power loop design. This is due to the much higher *di/dt* in the vertical design. As temperature increases, the *di/dt* is still fast enough for the detection time to converge to the propagation delay of the ICs. It is not until the junction temperature reaches 100 °C that the *di/dt* slows down enough to impact the detection time.

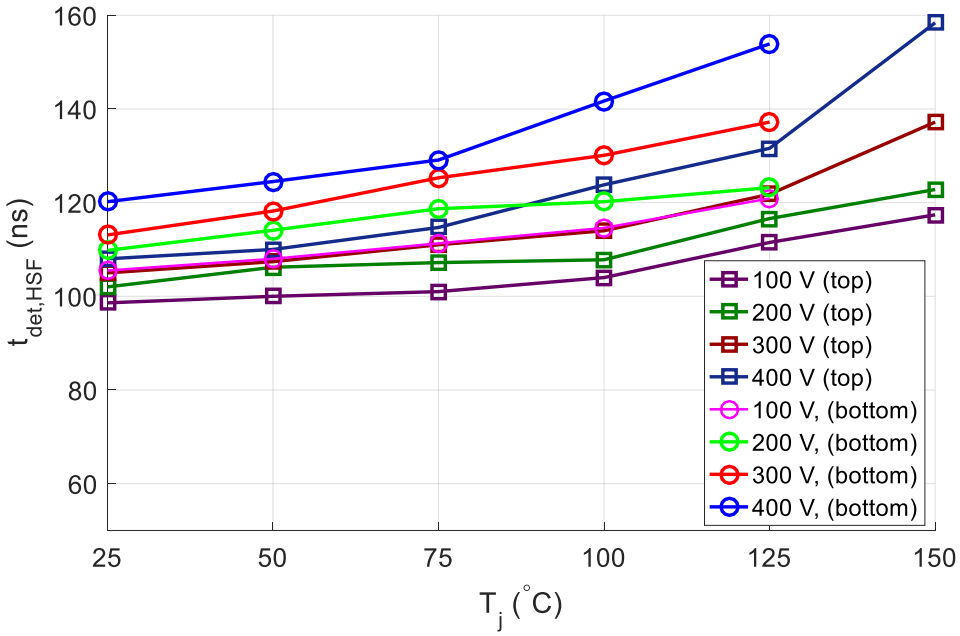


Figure 5.6. Comparison of HSF detection time between IGT60R070G1 (bottom-cooled) and IGOT60R070D1 (top-cooled) designs.

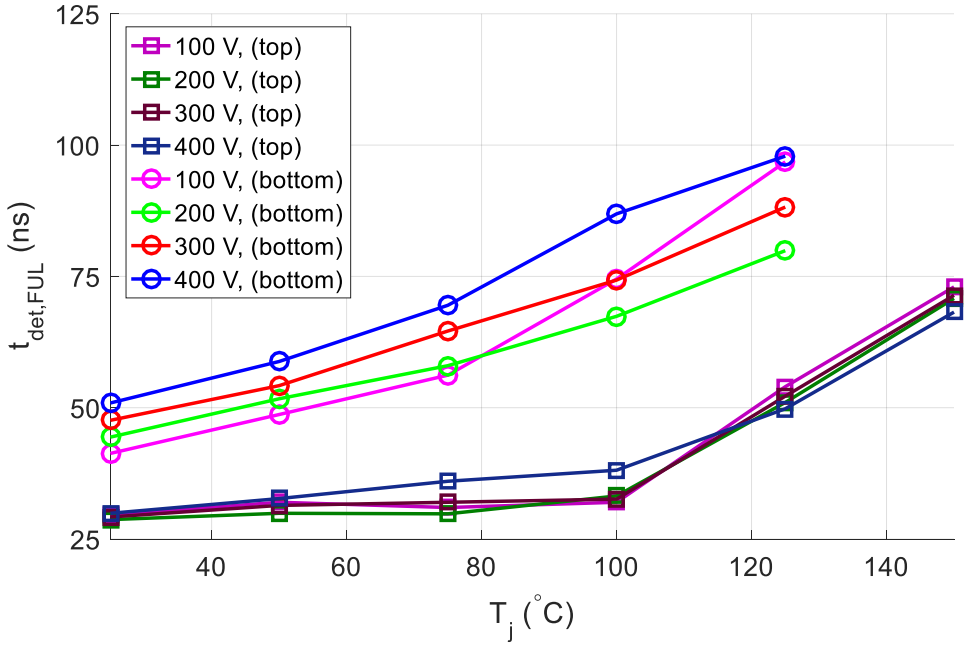


Figure 5.7. Comparison of FUL detection time between IGT60R070G1 (bottom-cooled) and IGOT60R070D1 (top-cooled) designs.

5.4 Consideration of circuit parameters

The results in [17] were all conducted with V_{dr} = 10 V, C_{su} = 1 nF, and R_{on} = 10 Ω for the gate drive circuit shown in Figure 3.15 (a), resulting in a turn-on *di/dt* of 10 A/ns. R_{ig} was set to supply a gate current of 25 mA. A blanking time of 40 ns was achieved utilizing the 80 pF equivalent junction capacitance of diodes *D1* and *D2* and an R_{lim} of 500 Ω. While these parameters were sufficient in protecting the devices, the impact of changing these parameters will be explored in this section. For example, the gate driver parameters impact the turn-on *di/dt*, which will either increase or decrease the detection time. The RC sensing circuit will impact the blanking time, which will affect both detection time and switching loss. And while the gate current is very small, this gate current setting will dictate the appropriate reference voltage, V_{ref}, responsible for setting the fault threshold current. Therefore, this section explores the impact of various parameters on the performance of the protection circuit in order to optimize the design for low switching loss, sufficient noise immunity, and fast detection time.

5.4.1 Impact of gate drive parameters

In Chapter 3, the driving voltage, V_{dr}, and series capacitance, C_{su}, were varied over the full operating range in order to choose a combination of parameters that result in low switching loss and overshoot voltage. In the first phase of the protection scheme, a 10 V drive with 1 nF series capacitance was utilized, resulting in ~10 A/ns *di/dt*, which was the fastest speed possible for the bottom-cooled design due to the high, lateral power loop inductance. However, the lower inductance of the vertical power loop design allowed the *di/dt* to be increased.

Figure 5.8 and Figure 5.9 show the impact of varying *di/dt* on the protection detection time and short-circuit energy. As expected, for the HSF case, the detection time decreases linearly with the turn-on *di/dt*. Additionally, there is decrease in ~0.5 mJ from 8.5 A/ns to 12 A/ns gate drive speed. However, the impact of the turn-on *di/dt* on the FUL detection time is not significant. During a FUL, the main limiting factor of the *di/dt* is the power loop inductance, not the the gate drive speed. In the vertical design, L_{loop} is ~6 nH with the shunt resistor, and detection time converges to the propagation delay of the ICs. This is a desirable property in that both devices in the phase leg of the full-scale converter will be implemented with the protection scheme. Therefore, during a fault, it is likely that either one of the devices will experience the FUL case, and that device will be turned off before the protection of the HSF device triggers.

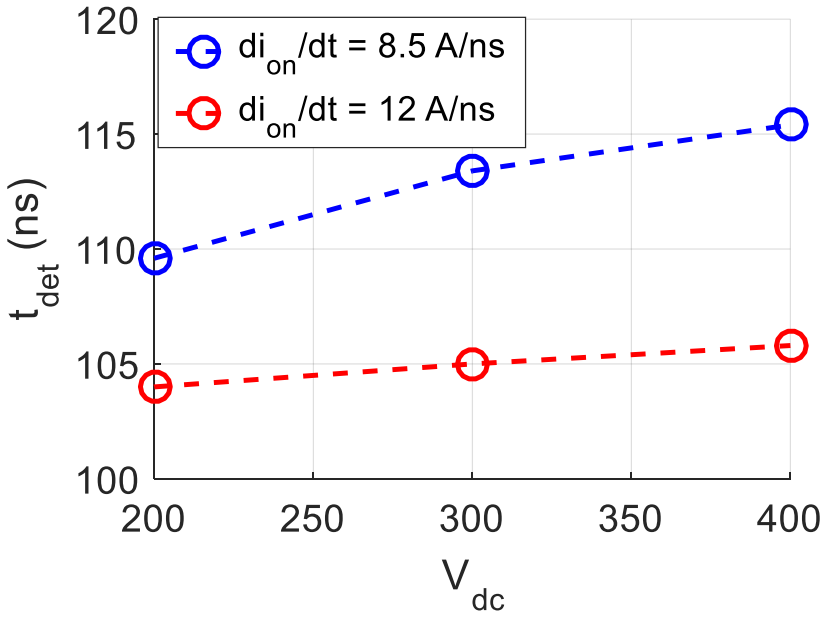


Figure 5.8. Impact of turn-on di/dt on HSF detection time.

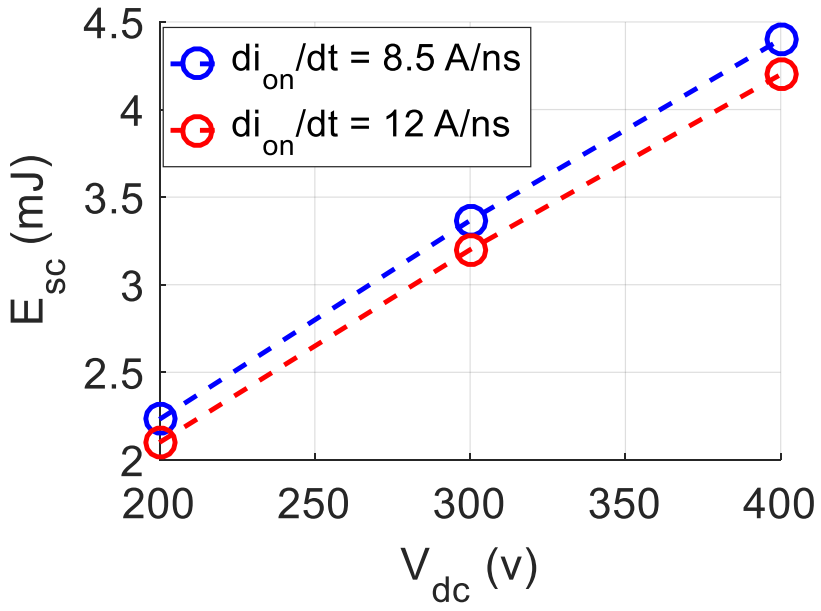


Figure 5.9. Impact of turn-on di/dt on HSF short-circuit energy loss.

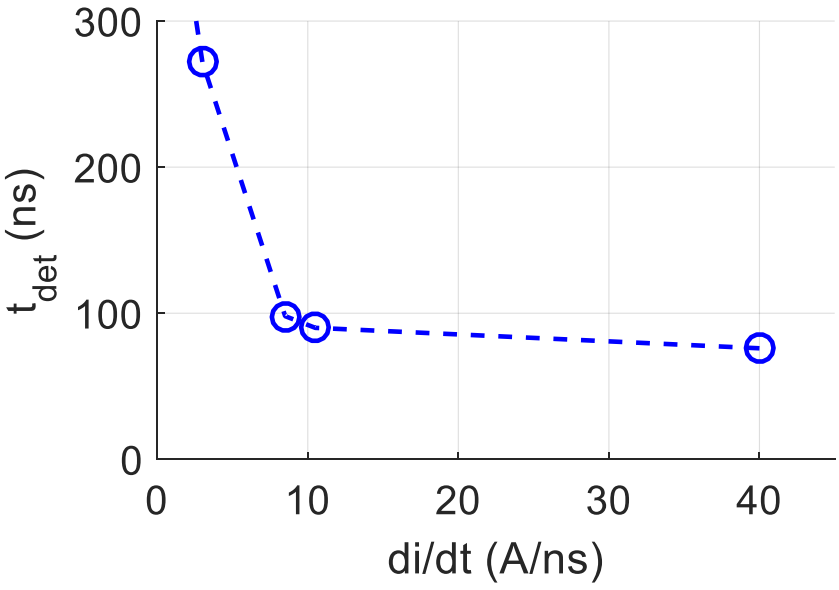


Figure 5.10. Impact of di/dt on detection time

5.4.2 Impact of current limiting resistor

For the initial implementation of the protection scheme, an R_{lim} of 500 Ω was utilized. The 80 pF equivalent capacitance of diodes *D1* and *D2* resulted in a blanking time of 40 ns. A sufficient blanking time is necessary to filter the initial turn-on transient of the device and to ensure sufficient noise immunity during continuous operation. However, it has been shown in previous sections that the protection time should be less than 200 ns with preferably as much margin as possible, as the device was also shown to fail after turn-off. Therefore, the blanking time should be as small as possible yet long enough to allow for sufficient noise immunity. In addition to adjusting the blanking time, the R_{lim} resistor also limits the current drawn by the comparator circuit, meaning the higher the resistance, the less impact of the protection circuit on the switching loss. In this section, the impact of R_{lim} on detection time, short-circuit energy, and switching loss is studied.

Diodes *D1* and *D2* remained the same while the resistance was swept from 300-1000 Ω, resulting in a blanking time of 25-80 ns. The bus voltage was varied from 200-400 V with a turn-on *di/dt* of 12 A/ns. First, the DPT was implemented over the full operating range to test for noise immunity as blanking time is varied. From this test, it was concluded that a blanking time of 25 ns was not sufficient to filter the initial turn-on transient and resulted in a false triggering of the protection scheme. The minimal blanking time was determined as 30 ns, cooresponding to 400 Ω limiting resistance. The results in Figure 5.11 and Figure 5.12 show the impact of R_{lim} on the turn-on and turn-off switching loss. There is a slight impact on turn-on switching loss, ~0.5 μJ increase per 100 Ω decrease

in R_{lim}, and no impact on turn-off loss. It was also observed that the slower the turn-on *di/dt*, the higher the impact of R_{lim} on switching loss.

Next, R_{lim} was varied from 400-750 Ω over the full range of bus voltage with a turn-on *di/dt* of 12 A/ns. However, with an R_{lim} of 750 Ω, the corresponding blanking time of 60 ns was too long, and the device failed at 400 V after ~215 ns. Therefore, the detection time results shown in Figure 5.13 and Figure 5.14 include only up to 500 Ω R_{lim}. By decreasing R_{lim} from 500 Ω to 400 Ω, the detection time is decreased by 30-35 ns although the blanking time is only decreased by 10 ns. However, because the minimal blanking time is 30 ns, the recommended R_{lim} is 500 Ω to allow some margin to filter initial turn-on transient. Additionally, as turn-on *di/dt* is increased, R_{lim} must also increase.

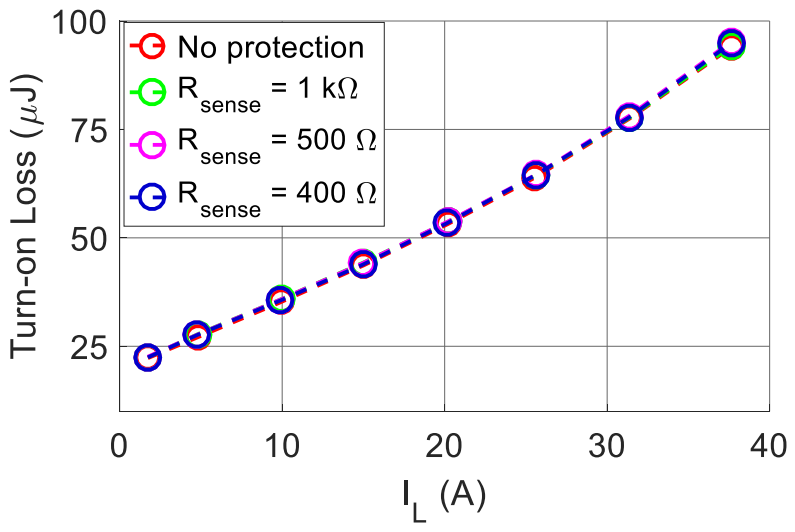


Figure 5.11. Impact of R_{sense} on turn-on switching loss for V_{dc} = 400 V.

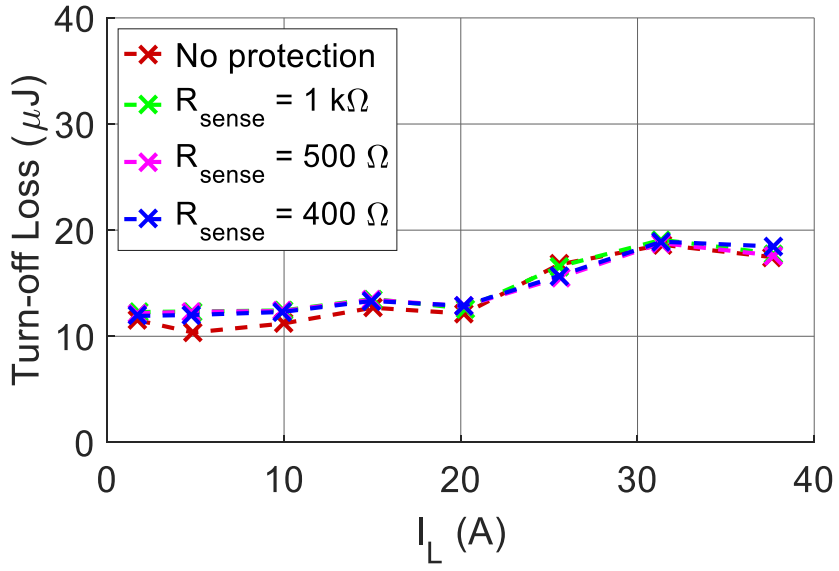


Figure 5.12. Impact of R_{sense} on turn-off switching loss for V_{dc} = 400 V.

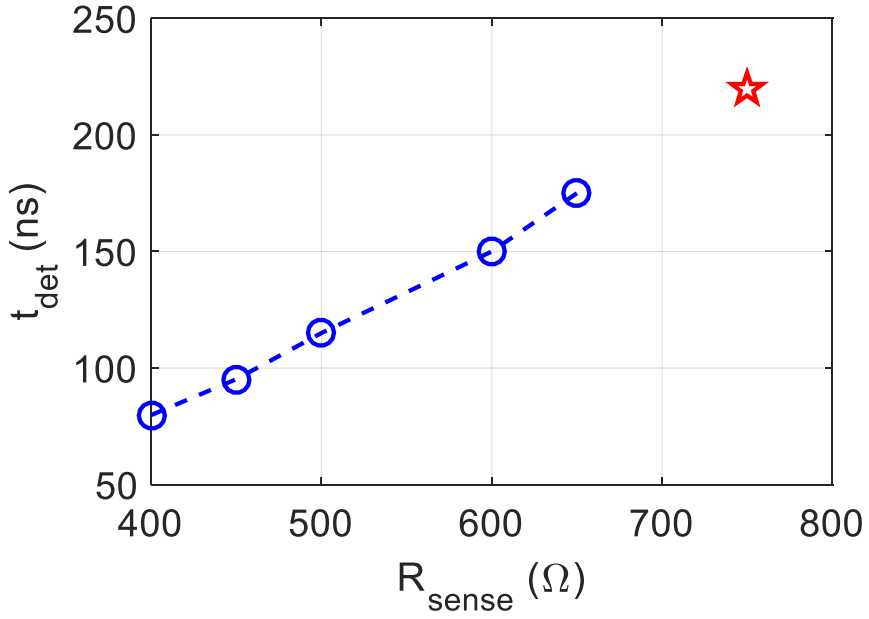


Figure 5.13. Impact of R_{sense} on HSF detection time for V_{dc} = 400 V with failure at R_{sense} = 750 Ω.

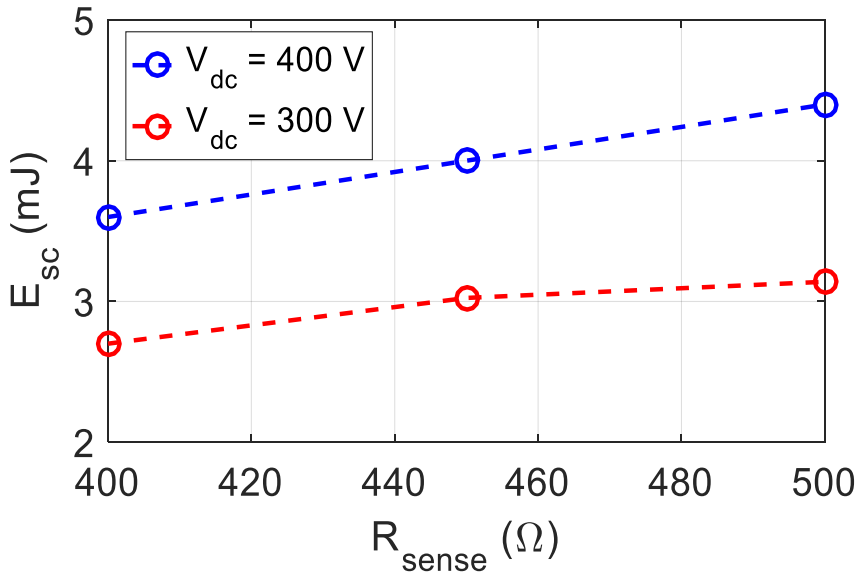


Figure 5.14. Impact of R_{esnse} on HSF short-circuit energy loss for V_{dc} = 300-400 V.

5.4.3 Impact of gate current

For initial design testing, the gate current was ignored in the external gate voltage calculation, which is responsible for determining the proper reference voltage for the chosen fault current threshold. However, further investigation shows that a change in gate current will have significant impact on fault threshold current if the reference voltage is not adjusted accordingly. The results in Figure 5.15 show that for a fixed reference voltage, the drain current will increase 1.5 A per 1 mA change in gate current. This means that the reference voltage will need to be adjusted in order to maintain a fixed fault threshold current. Therefore, the gate current in (5.3) cannot be ignored in the design.

$$V_{gs} = V_{gs,diode} + (I_d + I_g)\, r_1 \ . \tag{5.3}$$

5.5 Impact of gate-sensing vs. desaturation protection on switching loss

Desaturation protection has shown to protect GaN devices as fast as 200 ns [76-78]. However, it has already been shown that the GaN device can fail after 215 ns of sustained short-circuit, leaving little margin if utilizing desaturation protection. The gate-sensing protection scheme, however, was shown to protect the devices in less than 160 ns at 400 V and 150 °C with a fast enough gate drive, and with both devices implementing protection, it is likely the protection time will be less than 100 ns for the FUL device. In addition to faster protection time, the gate-sensing scheme for the GIT allows the fault threshold current be selected independent of junction temperature, whereas desaturation protection is based on device saturation. This means that the fault current must be set much higher at room temperature in order to protect the device at higher junction temperature.

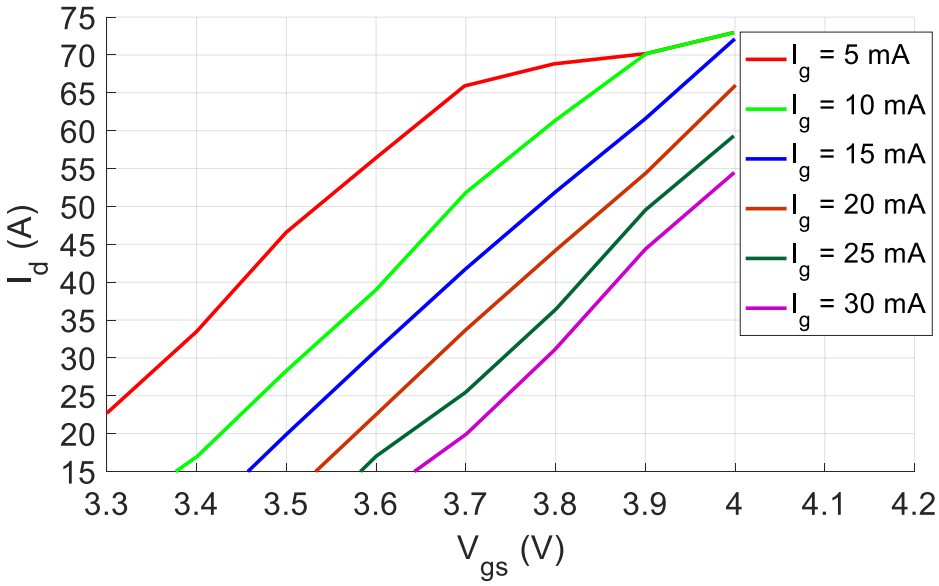


Figure 5.15. Impact of gate current on I_d-V_{gs} characteristic.

Another drawback of desaturation protection is the large sensing diode required to block the bus voltage. The junction capacitance of this diode adds to the parasitic output capacitance of the device, which will consequently increase the switching loss. The gate-sensing scheme, on the other hand, eliminates this C_{oss} loading but instead loads C_{gs}. However, the higher the blanking resistor, R_{lim}, the less the impact of the comparator circuit on switching loss. This section compares the impact of both circuits on the switching loss during normal operation to further verify the benefit of the gate-sensing circuit for the GIT over desaturation protection.

A DPT board was designed with the desaturation protection circuit shown in Figure 5.16. A 1 kV, fast recovery sensing diode, D_{dsat}, with a typical junction capacitance of 10 pF was utilized. A common diode size found in literature for 600 V level devices was between 10-30 pF junction capacitance. For this test, the smallest diode necessary was chosen. From the I-V characteristics shown in Figure 5.17, in order to achieve a fault threshold current of 35 A at elevated junction temperature, the reference voltage should be set to 5 V. However, at room temperature, that results in a fault current up to 65 A, which may result in insufficient protection time.

The DPT was performed from 300-500 V for both designs utilizing the gate-sensing scheme and the desaturation scheme, and the impact on switching loss was compared. It can be seen in Figure 5.11 that utilizing a 400 Ω current limiting resistance in the gate-sensing scheme contributes up to 1 μJ additional hard-switching loss.

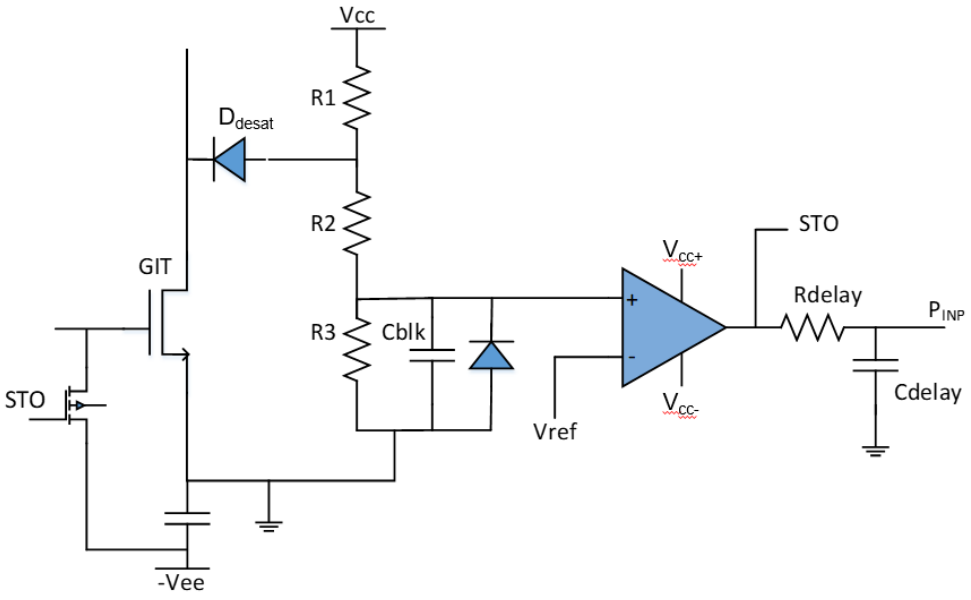


Figure 5.16. Desaturation protection schematic for GaN GIT.

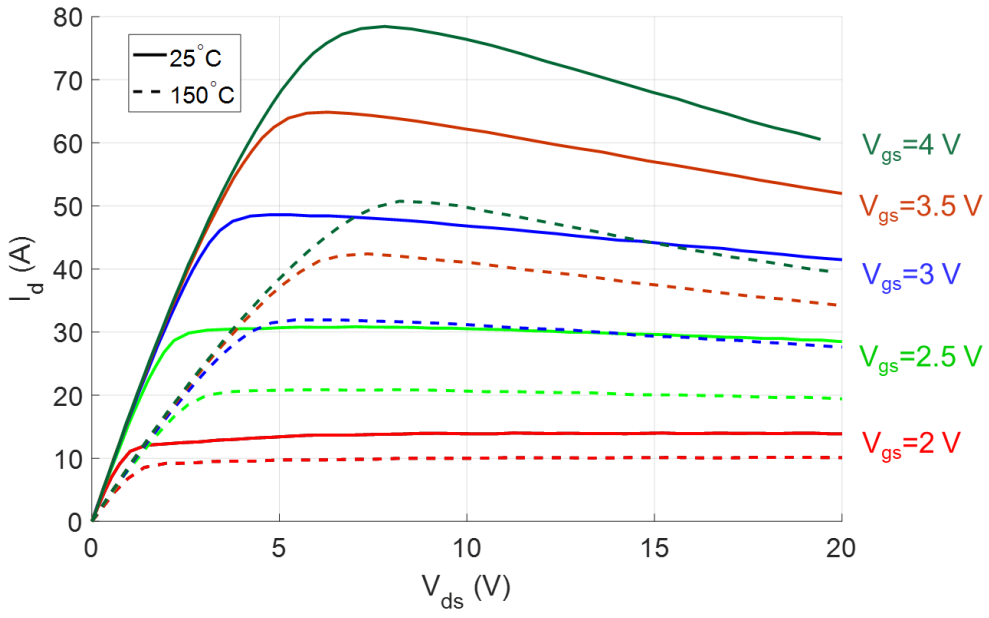


Figure 5.17. Output I-V characteristics for 600 V/30 A GaN GIT.

Desaturation protection should contribute additional loss that is $\frac{1}{2}\cdot C\cdot V^2$. For a 10 pF sensing diode, this would contribute 1.6 μJ additional switching loss if both devices in the phase leg implement the protection. According to the experimental results for one device in Figure 5.18, the additional switching loss measured is ~0.85 μJ for one device. Theoretically, the additional energy from the upper device would contribute an additional 0.8 μJ. While the difference additional switching loss is 0.5 μJ higher with desaturation protection, the impact on total converter loss is insignificant. Therefore, the main contribution of the gate-sensing protection scheme is the fast protection time and the ability to set fault threshold independent of junction temperature.

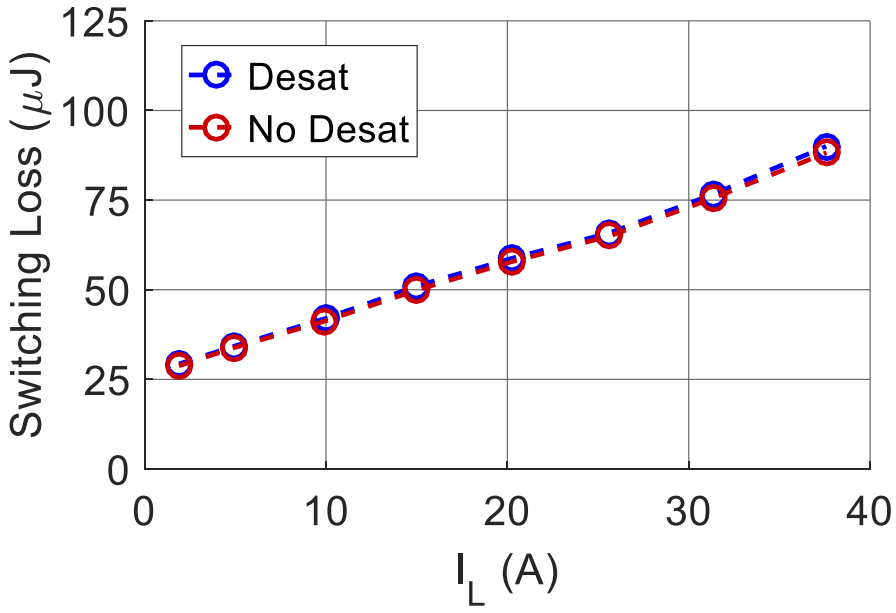


Figure 5.18. Impact of desaturation protection on switching loss.

5.6 Summary

The short-circuit robustness of the 600 V/30 A GaN GITs were tested at 400 V, revealing a similar critical energy for both device packages, ~6 mJ. The short-circuit withstand time before destruction was 215 ns, meaning protection should aim to turn devices off in less than 200 ns for safety margin. Failure waveforms indicate destruction of gate-drain and/or device channel at the time of failure due to an increase in leakage current and localized heating. Eventually, the gate-source also fails although in some cases this failure occurs some finite time after the initial failure. Testing at higher temperature revealed an increase in short-circuit robustness due to the decrease in saturation current and most likely a more uniform temperature distribution. Therefore, the assumed worst case condition is 400 V bus voltage at room temperature. However, the gate-sensing overcurrent protection scheme for GaN GITs was proven to successfully protect the devices up to 400 V and 150 °C junction temperature. Packaging of the top-cooled device proved to cause undesirable oscillations at high current that eventually resulted in overvoltage destruction. The thermal pad was soldered directly to the source pins to provide a low-resistance path for the high current, which eliminated the oscillations. Finally, the effect of both desaturation protection and gate-sensing protection on switching loss was determined to be insignificant, although it is likely that the gate sensing scheme is faster than desaturation protection judging by the literature. However, this is a piece of future work necessary to do full comparison of the performance of both schemes.

Chapter 6

Conclusion

6.1 Summary

a) Static characterization methodology was presented for gate current design that results in lowest R_{dson} and gate drive loss. Dynamic characterization of the GaN GIT was extended from [49] to include an extensive sweep of gate drive parameters over various operating conditions to determine an optimal trade-off between switching loss and overshoot voltage. The trade-off was compared between two designs: one implementing a lateral power loop layout and the other a vertical power loop layout. The results show that despite the larger package parasitics of the top-cooled device, the vertical power loop layout reduced the power loop inductance from 13 nH to 6 nH, which allowed the gate drive speed to increase from 10 A/ns to 17 A/ns while maintaining an overshoot voltage below the device 600 V rating. Considering the shunt resistor adds ~3 nH inductance to the power loop, the gate drive speed can increase further. The switching loss in Phase 2 converter was reduced by 20% by increasing the gate drive speed, while the voltage overshoot increased by less than 5%. However, the switching loss induced in the top-cooled package is still higher than the bottom-cooled due to package gate parasitics. Despite this, the top-cooled package results in other overall converter benefits, such as more efficient cooling and lower conduction loss. A comparison of results to full-scale converter testing also revealed the importance of V_{ds} measurement method. Even a small increase in trace length can have significant

impact on the voltage measurement, and this should be taken into consideration when observing DPT results.

b) The impact of negative gate voltage and various dead times on cross-talk and converter loss were explored in Chapter 4. Testing revealed that dead time loss for a lateral device like the GaN GIT can contribute up to 40% additional switching loss depending on the dead time and the operating condition. A model based on experimental results was developed for optimal dead time vs. instantaneous load current, which can achieve zero dead time loss when implemented as an adaptive dead time scheme. Compared to utilizing a fixed dead time, an adaptive scheme can save up to 15% total converter loss, mostly in light load current conditions where switching loss dominates the conduction loss. Calculation of fixed dead time loss vs. RMS load current was then used to determine an optimal fixed dead time based on operating conditions. For an application such as a PV inverter, where the operating condition can change over a wide range, an optimal fixed dead time is not possible, and a trade-off study of loss over the entire operating range can be conducted to determine an appropriate fixed dead time.

c) In Chapter 5, the overcurrent protection scheme for GaN GIT discussed in [17] with a bottom-cooled package of the 600 V/30 A GaN GIT was implemented on the top-cooled package of the same device, and the performance of the protection scheme was compared between the two. The study included a short-circuit robustness test of the device in both packages, and the results show that the critical energy is the same for both. At 380 V, the critical energy is ~7 mJ after 315 ns, whereas at 400

V, the critical energy drops to 6 mJ after 215 ns. Only a 20 V increase in bus voltage resulted in a 100 ns reduction in destruction time and 1 mJ reduction in critical energy. Comparison of protection performance for both devices over various operating conditions and junction temperatures show an improvement in performance when implementing the top-cooled device. Because the detection time of the protection scheme is dependent on the *di/dt*, a reduction in power loop inductance by half improves detection time by up to 50 ns in FUL case, whereas the HSF detection time is reduced by 20 ns due to the ability to increase gate drive speed. An extended study of the impact of protection circuit parameters was conducted to determine impact of gate drive speed and current limiting resistor, R_{lim}, on detection time and switching loss. A lower resistance will result in faster blanking time, but noise immunity and switching loss will suffer. However, a higher resistance will result in slower blanking time, and due to the small time margin necessary to protect the devices during short circuit, the study reveals that at least 35-40 ns blanking time is necessary, which will result in ~1 μJ additional switching loss.

6.2 Future work

Future work in this area may include the following:

a) The results in Chapter 3 reveal increase in overshoot voltage as R_{off} increases. While gate driver delay may partially explain this phenomenon, comparing switching performance using a different gate driver could prove beneficial. Double pulse testing also revealed interesting differences in switching performance

between different board designs that may be explored further to explain physically, such as the higher switching loss induced in the top-cooled device. Exploration of package and PCB parasitics should be explored. One concern in DPT is proper measurement of voltage and current waveforms. Although a standard BNC connector is used to measure the V_{ds} of the device, the length and position of PCB traces for the BNC connector may impact the measurement and the final switching loss calculation. However, differences in current waveforms, particular during the turn-on transient and during C_{oss} charging and discharging, were observed, and it would be beneficial to understand the cause since switching loss is affected. Differences in device package and PCB parasitics are likely the cause, and device modeling and simulation can help discover this difference in behavior.

b) This leads to device modeling of the GIT as a potential topic for future work. A model of switching loss and overshoot voltage as a function of capacitive gate drive parameters will be very beneficial as double pulse testing and sweeping of parameters is very time consuming. It will also allow a more extensive sweep of parameters to be accomplished with a sufficient physical model of the device.

c) Dead time loss model based on experimental results was developed in Chapter 4. Future work will include developing an analytical model based on device parameters and gate drive parameters. The loss model is also based on bipolar power supply. Dead time loss with unipolar supply using the capacitive gate drive scheme may be compared to the bipolar supply method. Is the difference significant? An adaptive dead time model was also developed without

implementation in the full-scale converter. Adaptive dead time schemes have been implemented on lower voltage level converters, but other challenges will be met in higher power converters, particularly in inverter operation. This is due to high *dv/dt* noise and a lack of simple and accurate sensing techniques. In inverter operation, implementation is further complicated by the fast-changing instantaneous load current at high switching frequency. However, testing of the model in the converter will determine what are the challenges and how to overcome them. The impact of power factor on loss is also a topic for future work. Although the converter tested in this work utilizes a purely resistive load, the experimental results presented can be used to evaluate the loss for other power factors as the loss vs. instantaneous load current will not change, but the average loss will change.

d) The protection scheme in Chapter 5 will be implemented in the full-scale converter to verify performance in a higher noise environment. Future work should also include implementation of the protection scheme on different GIT devices of various voltage and current ratings to verify practicality. Finally, a full comparison of desaturation protection to the gate-sensing scheme should be conducted to verify the benefit of the gate sensing scheme. Protection time and impact on system behavior should be considered.

6.3 Publications

- P. Williford, E. Jones, Z. Yang, J. Chen, F. Wang, S. Bala, and J. Xu, “Optimal Dead time Setting and Loss Analysis for GaN-based Voltage Source Converter,”

IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 898-905

Co-authored publications:

- E. A. Jones, P. Williford, Z. Yang, J. Chen, F. Wang, S. Bala*, et al.*, "Maximizing the voltage and current capability of GaN FETs in a hard-switching converter," in *2017 IEEE 12th International Conference on Power Electronics and Drive Systems (PEDS)*, 2017, pp. 740-747.E.
- A. Jones, P. Williford, and F. Wang, "A fast overcurrent protection scheme for GaN GITs," in 2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), 2017, pp. 277-284.

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Vita

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